CLASS TEST

S.No.: 01_SK_CS_BCD_20022025

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DIGITAL LOGIC

COMPUTER SCIENCE & IT

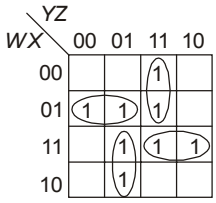
Date of Test : 20/02/2025

ANSWER KEY ➤

1.	(b)	7.	(c)	13.	(a)	19.	(a)	25.	(c)
2.	(c)	8.	(c)	14.	(c)	20.	(d)	26.	(d)
3.	(c)	9.	(b)	15.	(b)	21.	(c)	27.	(c)
4.	(d)	10.	(c)	16.	(c)	22.	(a)	28.	(d)
5.	(b)	11.	(a)	17.	(a)	23.	(b)	29.	(b)
6.	(d)	12.	(d)	18.	(b)	24.	(d)	30.	(a)

DETAILED EXPLANATIONS

1. (b)



$$Z = \bar{W}X\bar{Y} + WXY + \bar{W}YZ + W\bar{Y}Z$$

2. (c)

The worst case is when all 10 flip-flops are complemented.

The maximum frequency is $\frac{10^9}{30}$ = 33.3 MHz

3. (c)

$(x - 3)(x - 6) = x^2 - (6 + 3)x + 6 \times 3 = x^2 - 11x + 22$

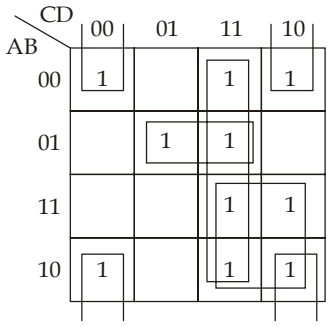
$(6 + 3)_{10} = (11)_b$

$9 = b + 1$

So, $b = 8$

Also, 6 × 3 = (18) in base 10 = (22) in base 8.

4. (d)

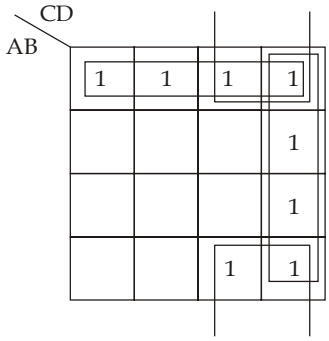


Minimized expression = CD + B′D′ + AC + A′BD

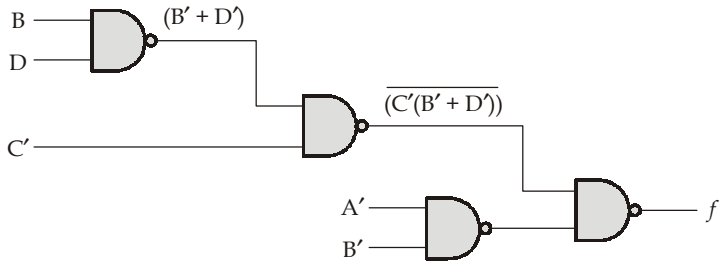
Number of literals is counting number of variables in the expression.

Thus, 2 + 2 + 2 + 3 = 9

5. (b)



$$F = A'B' + B'C + CD'$$
$$F = A'B' + C(B' + D')$$



Therefore we need 4 NAND gates.

6. (d)

Given, $T_c = 20$ ns and $T_s = 40$ ns

$$\left.\begin{aligned} T_{s0} &= 40 \text{ ns} \\ T_{s1} &= (40+20)\text{ns} = 60 \text{ ns} \\ T_{s2} &= (60+20)\text{ns} = 80 \text{ ns} \\ T_{s3} &= (80+20)\text{ns} = 100 \text{ ns} \end{aligned}\right\}$$

Since final sum result takes 100 ns, therefore rate of addition per second = $\frac{1}{100 \text{ ns}} = (10)^7$.

7. (c)

Given, Binary number = $\underset{\text{MSB}}{1}1011011$

- In signed-magnitude representation first bit representation sign so, it is negative number because MSB is 1.

$\Rightarrow$ $\underset{\_}{1}1011011 = -91$

- In 2's complement

$111011011 = -(00100101)_2 = -37$

8. (c)

Let the output of XNOR gate is Y.

$$Y = [Q_3 \oplus Q_1 \oplus Q_0] \odot Q_5$$

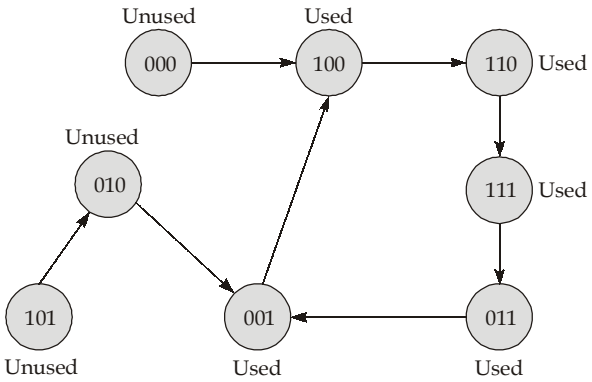
CLK	Y	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
–	–	1	0	0	0	0	0
1	0	0	1	0	0	0	0
2	1	1	0	1	0	0	0
3	1	1	1	0	1	0	0
4	0	0	1	1	0	1	0

9. (b)

$$Q_{3N+1} = J_3\bar{Q}_{3N} + \bar{K}_3Q_{3N}$$
$$= \bar{Q}_{2N}\bar{Q}_{3N} + \bar{Q}_1Q_{3N}$$

$$Q_{2N+1} = J_2\bar{Q}_{2N} + \bar{K}_2 Q_{2N} = Q_{3N}\bar{Q}_{2N} + Q_{3N}Q_{2N} = Q_{3N}$$
$$Q_{1N+1} = J_1\bar{Q}_{1N} + \bar{K}_1 Q_{1N}$$
$$= Q_{2N}\bar{Q}_{1N} + Q_{2N}Q_{1N} = Q_{2N}$$

Present state			Next state		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1

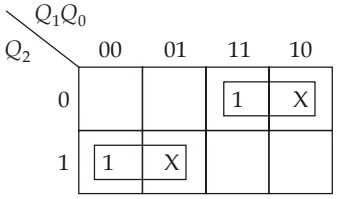


10. (c)

- Number of unused states in Johnson counter is $2^n - 2n$.

11. (a)

Present State			Next State			T_2
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	X	X	X	X
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	1	X	X	X	X
1	1	0	1	0	0	0
1	1	1	1	1	0	0



$$T_2 = Q_2 \oplus Q_1$$

12. (d)

In ripple counter using J-K flip-flop with positive edge triggered, the output of one FF is fed as clock input the next FF. All FF are fed with inputs.

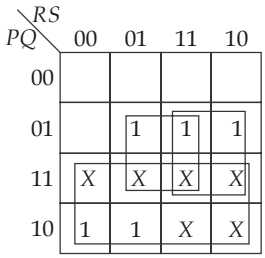
Hence the option (d) is correct

13. (a)

Truth table for BCD to excess-3 code output:

Decimal Value	Input				Output				Decimal Value
	P	Q	R	S	P	Q	R	S	
0	0	0	0	0	0	0	1	1	3
1	0	0	0	1	0	1	0	0	4
2	0	0	1	0	0	1	0	1	5
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
5	0	1	0	1	1	0	0	0	8
6	0	1	1	0	1	0	0	1	9
7	0	1	1	1	1	0	1	0	10
8	1	0	0	0	1	0	1	1	11
9	1	0	0	1	1	1	0	0	12

K-map for P: $f(P, Q, R, S) = \Sigma m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$



$= P + QS + QR$

$= P + Q(S + R)$

14. (c)

We consider the last full adder far worst case delay.

Time after which output carry bit becomes available from the last full adder.

= total number of full address × carry propagation delay of full adder.

$= 16 \times 12 \text{ ns} = 192 \text{ ns}$

Time after which output sum bit becomes available from the last full adder.

= time taken for its carry in to become available + sum propagation delay of full adder.

= {total number of full address before last full adder × carry propagation delay of full adder} + sum propagation delay of full adder.

$= \{15 \times 12 \text{ ns}\} + 15 \text{ ns} = 195 \text{ ns}$

15. (b)

$(11X1Y)_8 = (12C9)_{16}$

$001001\ X\ 001\ Y = 0001\ \underbrace{0010}_{X}\ 1100\ \underbrace{1001}_{Y}$

These are missing in left side. Hence $X = 3$ and $Y = 1$.
So, $X + Y = 3 + 1 = 4$

16. (c)
Statement I, II and III are correct.

17. (a)
Single Precision Format

1-bit	8-bit	23-bit
Sign	Exponent	Mantissa

Sign = 1, so number is negative.

Exponent = 10001010 = 138
Actual exponent = 138 – 127 = 11 [∵ 127 is biased value]
Normalized Mantissa = $111\underbrace{000.....}_{20 \text{ times}}$

Actual value = $1.111\underbrace{00.....}_{20 \text{ times}}$

Decimal value = $-1.11100 ..... \times 2^{11} = -(111100000000)$
$= -(2048 + 1024 + 512 + 256) = (-3840)_{10}$

18. (b)

CLK	Q_0	Q_1	Q_2	$J_0\ K_0$	$J_1\ K_1$	$J_2\ K_2$	$\overline{Q}_1$	$\overline{Q}_2$ (2 input gate)
0	0	0	0	1 1	1 1	1 1	1	1
1	1	0	0	1 1	1 1	1 1	1	1
2	0	1	0	1 1	1 1	1 1	0	1
3	1	1	0	1 1	1 1	1 1	0	1
4	0	0	1	1 1	1 1	1 1	1	0
5	1	0	1	1 1	1 1	1 1	1	0
6	0	1	1	1 1	1 1	1 1	0	0

Now if we will use OR gate then the flip flop will be CLR and we will get mod-6 counter from (0 to 5).

19. (a)

Clock	$S.I = Y$	Q_3	Q_2	Q_1	Q_0
		0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	1	1	1	1	1
5	0	0	1	1	1

← Required Content

Total 5 clock cycles are required.

20. (d)
All the above statements are correct.

21. **(c)**

Normally, characteristic equation for *J-K* flip flop

$$Q_{n+1} = J_0 Q_n' + K_0' Q_n$$

Now here, $D = \overline{\overline{XQ_n} \cdot \overline{YQ_n'}} = XQ_n + YQ_n'$

where $X = K'$ and $Y = J$

So, option (c) is correct.

22. **(a)**

$$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

$$= \bar{A}\bar{B}C + \bar{A}B \cdot 1 + A\bar{B}1 + ABI_3 = \bar{A}\bar{B}C + \bar{A}B + A\bar{B} + ABI_3$$

$$= B(\bar{A} + AI_3) + \bar{B}(\bar{A}C + A)$$

$$= B(\bar{A} + I_3) + \bar{B}(A + C) \quad \ldots(i)$$

Let $I_3 = A$,

$$F = B(A + \bar{A}) + \bar{B}(A + C) = B + \bar{B}(A + C)$$

$$= (B + \bar{B})(A + B + C)$$

$$= A + B + C$$

Let $I_3 = C$,

$\therefore$

$$F = B(\bar{A} + C) + \bar{B}(A + C) = \bar{A}B + BC + A\bar{B} + C\bar{B}$$

$$F = \bar{A}B + C + A\bar{B} \neq A + B + C$$

Let $I_3 = 0$,

$\therefore$

$$F = B(\bar{A} + 0) + \bar{B}(A + C)$$

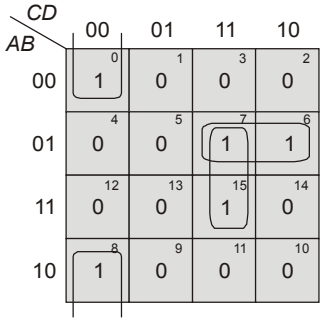
$$= \bar{A}B + A\bar{B} + \bar{B}C \neq A + B + C$$

23. **(b)**

$$f_1(A, B, C, D) = \Sigma m(0, 1, 5, 6, 7, 8, 15)$$

$$f_2(A, B, C, D) = \Sigma m(0, 2, 4, 6, 7, 8, 13, 14, 15)$$

$\therefore$ $f_3(A, B, C, D) = \Sigma m(0, 6, 7, 8, 15)$



There are 3 EPIs.

24. **(d)**

The output,

$$Y_0 = A_0 B_0$$

$$Y_1 = B_0 A_1 \oplus B_1 A_0$$

$$Y_2 = B_1 A_1 \oplus \text{Carry 1}$$

$$Y_3 = \text{Carry 2}$$

Thus, it can be seen that the output is equal to multiplication of 2-bit number $(A_1 A_0)$ and $(B_1 B_0)$.

25. (c)

$$f = \bar{S}_1 \bar{S}_0 \bar{I}_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Now, $S_1 = B, S_0 = A, I_0 = D, I_1$

$= (\overline{C+D}) = \bar{C}\bar{D}$, $I_2 = CD$ and $I_3 = 1$

$\therefore$ $f = \bar{B}\bar{A}D + \bar{B}A\bar{C}\bar{D} + B\bar{A}CD + AB$

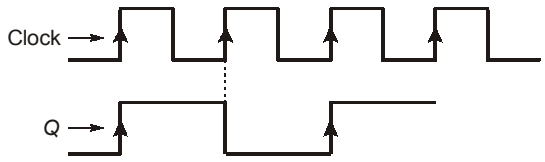
Expressing the boolean function in canonical form by using *K*-map, we get,

CD / AB	00	01	11	10
00	0 (0)	1 (1)	1 (3)	0 (2)
01	0 (4)	0 (5)	1 (7)	0 (6)
11	1 (12)	1 (13)	1 (15)	1 (14)
10	1 (8)	0 (9)	0 (11)	0 (10)

$f(A, B, C, D) = \Pi M\ (0, 2, 4, 5, 6, 9, 10, 11)$

26. (d)

J-K flip-flop is in toggle node so after every clock pulse output Q toggles. So output Q will be as



and Q is input to MOD-3 counter then

after 3 clock pulses of input clock there are 2 +ve edge of clock input Q so output of counter goes to 2 = $(10)_2$

So, $AB = 10$

So, Q, A and B respectively is 110.

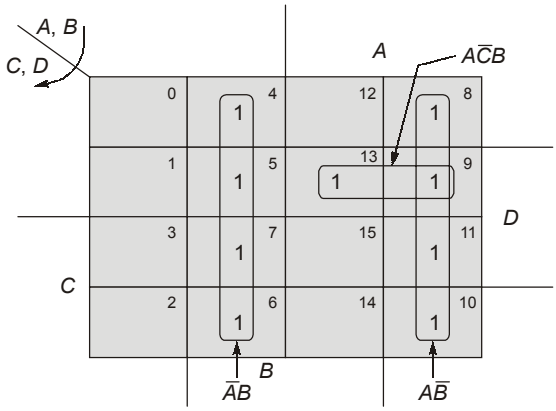
27. (c)

$$f(A, B, C, D) = \Sigma m\ (1, 4, 5, 8, 10, 12, 14, 15) \quad \ldots(1)$$

$$f_2(A, B, C, D) = \bar{A}B + A\bar{B} + A\bar{C}D$$

Identify the minterms using *K*-map for the function f_2.

$$f_2(A, B, C, D) = (4, 5, 6, 7, 8, 9, 10, 11, 13) \quad \ldots(2)$$



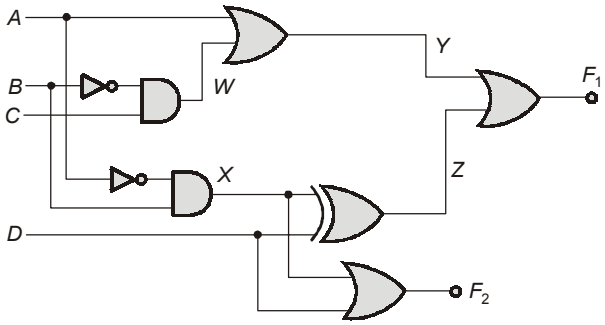
Compare equation (2) and (1) for common minterms.
Common minterms are (4, 5, 8, 10)
(4, 5, 8, 10) minterms are contributed to the function *f*, by the AND gate.

So that function $\overline{f}_3(A,B,C,D) = \Sigma m\ (1, 12, 14, 15) + d\ (4, 5, 8, 10)$

or $f_3(A, B, C, D) = \Pi m\ (1, 12, 14, 15) \cdot d\ (4, 5, 8, 10)$

Hence option (c) is correct.

28. (d)



The Boolean function at each stage of logic circuit

$W = \overline{B}C,\ X = \overline{A}B,\ Y = A + W = A + \overline{B}C$ and $Z = D \oplus X = D \oplus (\overline{A}B)$

$= \overline{A}B\overline{D} + D(A + \overline{B}) = \overline{A}B\overline{D} + AD + \overline{B}D$

$\therefore \quad F_1 = Y + Z$

$= A + \overline{B}C + \overline{A}B\overline{D} + AD + \overline{B}D$

$= A + \overline{B}C + B\overline{D} + \overline{B}D$

$\because \quad (A + AD = A,\quad A + \overline{A}B\overline{D} = A + B\overline{D})$

Similarly, $F_2 = X + D = \overline{A}B + D$

$\because \quad \overline{B} = 0$

We get, $F_1 + F_2 = A + \overline{A} + D + \overline{D} = 1$

29. (b)

Developing the state table, we get,

Present State	Next State		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	b	c	0	0
b	d	e	1	0
c	c	d	0	1
d	a	d	0	0
e	c	d	0	1

Same state

Hence the reduced state function

Present State	Next State		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	b	c	0	0
b	d	c	1	0
c	c	d	0	1
d	a	d	0	0

It is not possible to reduce the state diagram further. So, there are 4 states in the reduced state diagram. Minimum 2 flip-flops are required to design a circuit with 4 states.

30. (a)

State table can be drawn from state diagram:

Present state	Input	Next state
Q_n	X	Q_{n+1}
0	1	0
0	0	1
1	1	0
1	0	0

$Q_{n+1} = \overline{Q_n + X}$ (Q_{n+1} represent output of NOR gate)

■■■■