CLASS TEST — S.No.: 01SK_ECEE_ABC_200225

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DIGITAL ELECTRONICS

EC-EE

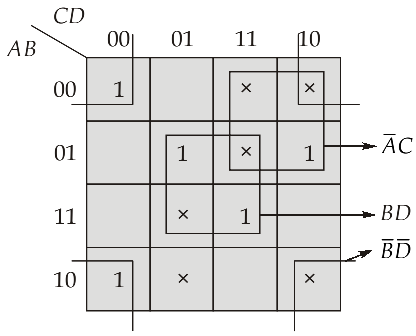
Date of Test : 20/02/2025

ANSWER KEY

1.	(c)	7.	(d)	13.	(b)	19.	(b)	25.	(a)
2.	(c)	8.	(a)	14.	(b)	20.	(c)	26.	(a)
3.	(b)	9.	(c)	15.	(b)	21.	(a)	27.	(c)
4.	(d)	10.	(c)	16.	(c)	22.	(a)	28.	(b)
5.	(c)	11.	(b)	17.	(c)	23.	(c)	29.	(c)
6.	(b)	12.	(b)	18.	(d)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

1. (c)



The function is $BD + \bar{B}\bar{D} + \bar{A}C$

2. (c)

$$\% \text{ Resolution} = \frac{1}{2^N - 1} \times 100\% = \frac{1}{2^4 - 1} \times 100\% = \frac{100}{15} = 6.67\%$$

3. (b)

Given that,

$$\begin{array}{r} 1011001111 \\ +1 \\ \hline 1011010000 \end{array}$$

Complemented output

$\therefore$ No. of flip flop = 5

4. (d)

The flip-flop is connected in toggle mode. Thus, $Q_{n+1} = \bar{Q}_n$.

5. (c)

The excitation table of a J-K flip-flop can be given as

Q_n	Q_{n+1}	J	K	
0	0	0	x	
0	1	1	x	
1	0	x	1	← Required excitation
1	1	x	0	

6. (b)

In the given digital circuit each multiplexer is working as a NOT gate thus it is a ring oscillator with five NOT gates. The frequency of oscillation will be $f = \frac{1}{2Nt_{pd}}$.

N = number of NOT gates in cascade

t_{pd} = propagation delay of each NOT gate.

$$\therefore \quad f = \frac{1}{2 \times 5 \times 25ns} = 4 \times 10^6 \text{ Hz} = 4 \text{ MHz}.$$

7. **(d)**

As A, B is the select line and C is the input,

	I_0	I_1	I_2	I_3
$\bar{C}$	0	(2)	(4)	(6)
C	1	(3)	5	(7)
	0	1	$\bar{C}$	1

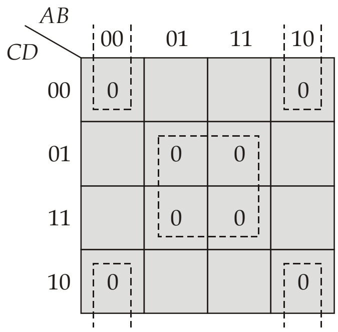
So, $\Sigma m\ (2, 3, 4, 6, 7)$ = Total no. of min-terms = 5

8. **(a)**

In general, the range of numbers that can be represented by an n-bit number with 2's complement representation is (-2^{n-1}) to $(+2^{n-1} - 1)$. The 2's compliment is the standard representation used for signed binary representation.

9. **(c)**

The Karnaugh map for POS form can be given by

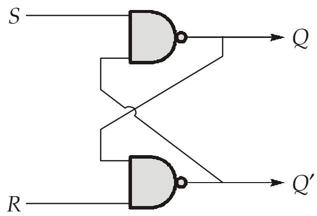


POS form of f is given as,

$$f(A, B, C, D) = (B + D)(\bar{B} + \bar{D})$$

10. **(c)**

SR latch by cross-coupling two NAND gates



NAND LATCH

If the both S and R inputs are set 0 then the result will be as follows:

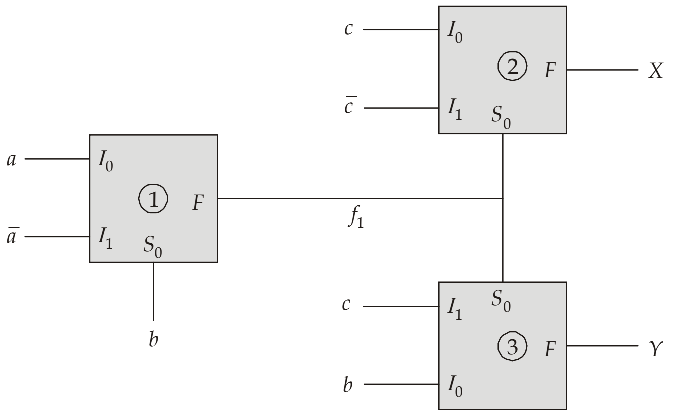
Truth table for the SR latch using the NAND gates

S	R	Q
0	0	Invalid state ($Q = Q' = 1$)
0	1	1
1	0	0
1	1	Previous state

$\therefore$ $Q = 1$

and $Q' = 1$

11. (b)



The output of 1st MUX, $f_1 = (a\bar{b} + \bar{a}b)$

Thus, Output $X = \overline{(a\bar{b} + \bar{a}b)}c + (a\bar{b} + \bar{a}b)\bar{c}$

$= a \oplus b \oplus c$

and Output $Y = \overline{(a\bar{b} + \bar{a}b)}b + (a\bar{b} + \bar{a}b)c$

$= ab + a\bar{b}c + \bar{a}bc = (ab + a\bar{b}c) + (ab + \bar{a}bc)$

$= a(b + \bar{b}c) + b(a + \bar{a}c) = ab + bc + ca$

So, the given circuit can act as a full-adder.

12. (b)

For $A = 1$,

$B = 0$

the output of ex-or gate will be 1.

So, $I_0 = 1$

$I_1 = 0$

$I_2 = B = 0$

$I_3 = A = 1$

$Y = \bar{C}\bar{D}I_0 + \bar{C}DI_1 + C\bar{D}I_2 + CDI_3 = \bar{C}\bar{D} + CD$

$Y = C \odot D$

13. (b)

Initial input to J_1K_1 will be 1 1

Input to J_0K_0 will be 1 0

After 1st clock pulse Q_0Q_1 will be 1 1

Input to J_1K_1 after 1st clock pulse will be 0 0

Input to J_0K_0 after 1st clock pulse will be 0 1

After 2nd clock pulse Q_0Q_1 will be 0 1

14. (b)

The *K*-map of the given function will be as shown below.

wx \ yz	00	01	11	10
00	0	0		x
01	0	0		
11				
10	0	0	0	x

So, $F(w, x, y, z) = (w+y)(\overline{w}+x)$

15. (b)

Present State		Next State		T_B	T_A
Q_B	Q_A	Q_B^+	Q_A^+		
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	1	1	0

$T_B = 1$; $\quad T_A = \overline{Q}_B\overline{Q}_A + \overline{Q}_B Q_A$

$T_A = \overline{Q}_B$

16. (c)

$$wx + w(x + y) + x(x + y) = wx + wx + wy + x + xy$$
$$= x(1 + y + w + w) + wy$$
$$= x + wy$$

∴ option (a) is correct

$$\overline{w\overline{x}(y+\overline{z})} + \overline{w}x = \overline{w\overline{x}} + \overline{y+\overline{z}} + \overline{w}x$$
$$= (\overline{w}+x) + (\overline{y}z) + \overline{w}x$$
$$= \overline{w} + x + \overline{y}z$$

∴ option (b) is correct

$$\left(w\overline{x}(y+x\overline{z}) + \overline{w}\overline{x}\right)y = \left(w\overline{x}y + w\overline{x}\cdot x\overline{z} + \overline{w}\overline{x}\right)y$$
$$= w\overline{x}y + \overline{w}\overline{x}y$$
$$= (w+\overline{w})\overline{x}y$$
$$= \overline{x}y$$

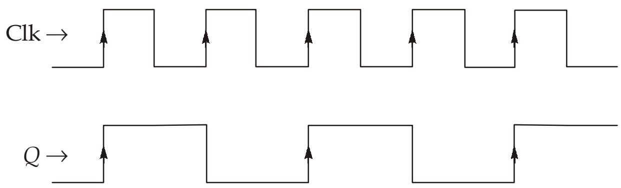
∴ option (c) is **incorrect**

$$(w + y)(wxy + wyz) = wxy + wyz + wxy + wyz$$
$$= wxy + wyz$$

option (d) is correct

17. (c)

J-K flip flop is in toggle mode so after every clock pulse output Q toggles so output Q will be as



and Q is clock to MOD-3 down counter then after 5 clock pulses of input clk there are 3 +ve edge of clock pulses applied to counter

∴ output of counter goes to

		A	B
Initially	→	0	0
1^{st} clk	→	1	1
2^{rd} clk	→	1	0
3^{rd} clk	→	0	1

∴ So the states of Q, A, B respectively are 101.

18. **(d)**

	A	B	Y	X	T_A
Initially	1	1	1	1	0
1^{st} CLK →	1	0	1	0	1
2^{nd} CLK →	0	0	0	1	1
3^{rd} CLK →	1	1	1	1	0
4^{th} CLK →	1	0	1	0	

∴ $(ABY)_2 = (101)_2 = 5$

19. **(b)**

$$Y = \overline{\overline{Q_1Q_3}\cdot\overline{Q_2Q_3}}$$

$$= Q_1Q_3 + Q_2Q_3$$

$$Y = Q_3(Q_1 + Q_2)$$

To reset the counter output Y must be one

$$Y = Q_3(Q_1 + Q_2)$$

Q_3	Q_2	Q_1	Q_0
1	0	1	0
1	1	0	0
1	1	1	0

when the counter output $Q_3Q_2Q_1Q_0$ = 1010. Then the output Y will give output 1 and it will be given to inverter, so it will reset the counter and again counting will start and it will not go for further combinations.

20. **(c)**

$$S = \left(\overline{P+Q} + \overline{P+\overline{P+Q}}\right)\left(\overline{P+\overline{P+Q}}\right)$$

Consider, $\overline{P+Q} = X$

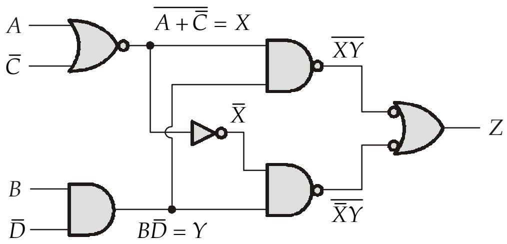
and $\overline{P+(\overline{P+Q})} = Y$

Then, $S = (X + Y)Y = XY + Y = Y$

$$S = \overline{P + (\overline{P + Q})} = \overline{P}\cdot(P+Q) = \overline{P}Q$$

So for, $S = 1$, P should be '0' and Q should be '1'.

21. (a)



$$Z = XY + \overline{X}Y$$
$$= Y = B\overline{D}$$

22. (a)

$$A\overline{C} + \overline{A}C = A(\overline{A\overline{B} + \overline{A}B}) + \overline{A}(A\overline{B} + \overline{A}B)$$
$$= A(\overline{A} + B)(A + \overline{B}) + \overline{A}A\overline{B} + \overline{A}\overline{A}B$$
$$= (A\overline{A} + AB)(A + \overline{B}) + \overline{A}B$$
$$= AB + AB\overline{B} + \overline{A}B$$
$$= AB + \overline{A}B$$
$$= B(A + \overline{A})$$
$$= B$$

Alternate Solution:

$$A\overline{B} + \overline{A}B = C = A \oplus B \text{ (Given)}$$
$$\overline{A}C + A\overline{C} = C = A \oplus C = A \oplus (A \oplus B)$$
$$= 0 \oplus B = B \qquad (\because A \oplus A = 0,\ 0 \oplus A = A)$$

23. (c)

$$S_1 = A \oplus B$$
$$C_1 = AB$$
$$S = (A \oplus B) \oplus AB$$
$$= (A \oplus B)\cdot\overline{AB} + \overline{(A \oplus B)}\cdot AB$$
$$= (A\overline{B} + \overline{A}B)(\overline{A} + \overline{B}) + (AB + \overline{A}\overline{B})(AB)$$
$$= A\overline{B} + \overline{A}B + AB = A + B$$
$$C = (A \oplus B)\cdot AB = (A\overline{B} + \overline{A}B)AB$$
$$= 0$$

Alternate Solution:

A	B	S_1	C_1	S $(S_1 \oplus C_1)$	C (S_1C_1)
0	0	0	0	0	0
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0

$\therefore$ $C = 0$

and $S = A + B$

24. **(b)**

Q_n	D	Q_{n+1}	Excitation inputs J	K
0	0	0	0	×
0	1	1	1	×
1	0	0	×	1
1	1	1	×	0

Excitation map for *J*

Q_n \ D	0	1
0	0	1
1	×	×

$J = D$

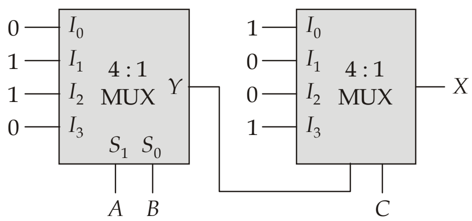
Excitation map for *K*

Q_n \ D	0	1
0	×	×
1	1	0

$K = \bar{D}$

25. **(a)**

We know,



$$Y = \bar{A}B + A\bar{B} = A \oplus B$$

$$X = Y \odot C = \overline{(\bar{A}\cdot B + A\bar{B})}\cdot\bar{C} + (\bar{A}\cdot B + A\bar{B})\cdot C$$

$$= \overline{(A \oplus B)}\cdot\bar{C} + \bar{A}\cdot B\cdot C + A\bar{B}C$$

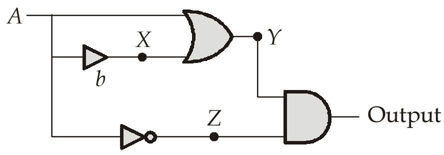
$$= (A \odot B)\bar{C} + \bar{A}\cdot BC + A\bar{B}C$$

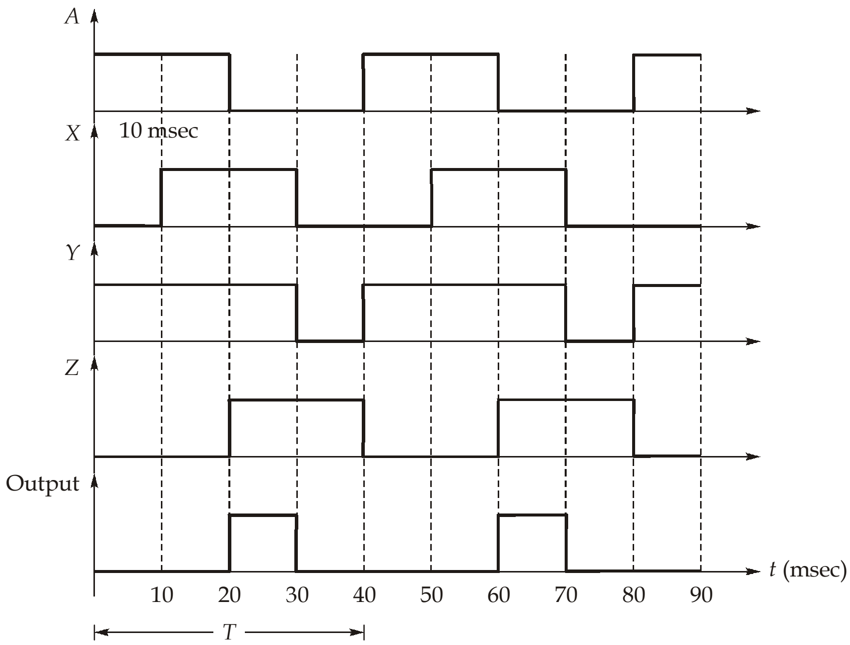
$$= (A\cdot B + \bar{A}\cdot\bar{B})\bar{C} + \bar{A}\cdot BC + A\bar{B}C$$

$$= A\cdot B\cdot\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\cdot B\cdot C + A\bar{B}C$$

26. **(a)**

Time period, $T = 40$ msec





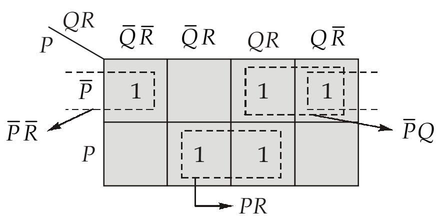
$$\text{Duty cycle of output wave} = \frac{10\text{m sec}}{40\text{m sec}} \times 100 = 25\%$$

27. **(c)**

Given, Boolean function,

$$F = m_0 + m_2 + m_3 + m_5 + m_7$$

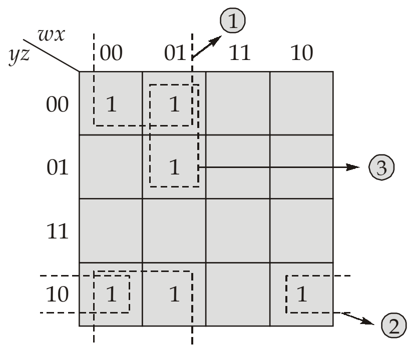
Using K-map for minimization



$$F = \bar{P}\bar{R} + \bar{P}Q + PR$$

28. (b)

$$f(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 10)$$



∴ 3 essential prime implicants.

29. (c)

By truth table

Number of clock pulse	$D_{in} = A \oplus D$	A	B	C	D
initial	–	1	1	0	1
1	0	0	1	1	0
2	0	0	0	1	1
3	1	1	0	0	1
4	0	0	1	0	0
5	0	0	0	1	0
6	0	0	0	0	1
7	1	1	0	0	0
8	1	1	1	0	0

Hence 8 clock cycles are required for state 1100.

30. (a)

Given configuration is MOD-10 up counter

$$\therefore \quad \text{Frequency at output} = \frac{\text{Clock frequency}}{10} = \frac{20\text{K}}{10} = 2 \text{ kHz}$$

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