REVISED ANSWER SHEET

Date: 07/12/2016

OFFLINE TEST SERIES

MADE EASY

India's Best Institute for IES, GATE & PSUs

ESE-2017 : Prelims Exam

UPSC Engineering Services Examination

E & T ENGINEERING

Answer Key & Solutions

Test 11: Part Syllabus Technical

Analog & Digital Electronics

1.	(a)	16.	(b)	31.	(a)	46.	(d)	61.	(c)
2.	(c)	17.	(a)	32.	(c)	47.	(d)	62.	(c)
3.	(d)	18.	(b)	33.	(b)	48.	(c)	63.	(c)
4.	(c)	19.	(c)	34.	(a)	49.	(b)	64.	(b)
5.	(c)	20.	(a)	35.	(b)	50.	(d)	65.	(c)
6.	(c)	21.	(c)	36.	(d)	51.	(a)	66.	(a)
7.	(c)	22.	(c)	37.	(a)	52.	(c)	67.	(d)
8.	(b)	23.	(b)	38	(c)	53.	(c)	68.	(d)
9.	(b)	24.	(b)	39.	(c)	54.	(a)	69.	(b)
10.	(b)	25.	(d)	40.	(d)	55.	(a)	70.	(c)
11.	(d)	26.	(a)	41.	(d)	56.	(d)	71.	(b)
12.	(b)	27.	(a)	42.	(b)	57.	(a)	72.	(c)
13.	(d)	28.	(c)	43.	(a)	58.	(c)	73.	(a)
14.	(c)	29.	(a)	44.	(c)	59.	(a)	74.	(d)
15.	(a)	30.	(c)	45.	(c)	60.	(c)	75.	(c)

* Answer Key & Explanation has been modified : Q.6

DETAILED EXPLANATIONS

1. (a)

Assuming both diodes are conducting

Applying KCL at the output node V_0, we get

$$\frac{V_0 - 10}{1} + \frac{V_0 - 5}{1} + \frac{V_0}{9} = 0$$

$$2V_0 + \frac{V_0}{9} = 15$$

$$\frac{19V_0}{9} = 15$$

$$\because \quad V_0 = \frac{15 \times 9}{19} = 7.10 \text{ V} > 5\text{V}$$

Thus diode D_2 will be OFF.

Hence, by voltage division rule $V_0 = \frac{10 \times 9}{10} = 9 \text{ V}$

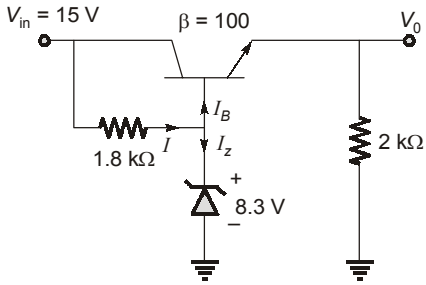
2. (c)

Clamper circuit is also known as DC restorer or DC reinserter.

3. (d)

For common collector or emitter follower amplifier voltage gain is nearly equal to unity.

4. (c)



$$I_z = I - I_B$$

$$= I - \frac{I_E}{(\beta + 1)}$$

$$= \left[\frac{15 - 8.3}{1.8} - \frac{(8.3 - 0.7)}{2(101)}\right] \text{mA}$$

$$\approx 3.7 \text{ mA}$$

5. (c)

The circuit shown in the figure represents a half-wave rectifier and for Half-wave rectifier circuit the conduction angle is $(\pi - 2\phi_i)$.

6. (c)

For a negative feedback amplifier

$$\frac{\partial A_f}{A_f} = \frac{1}{(1+A\beta)}\cdot\frac{\partial A}{A}$$

$$0.1 = \frac{1}{(1+100\beta)}\cdot(1)$$

$$0.1(1+100\beta) = 1$$

$$0.1 + 10\beta = 1$$

$$\beta = 0.09$$

8. (b)

$\because$ the input is a DC signal we can assume the capacitor for to be open circuited.

$$\Rightarrow \quad V_{out} = -\frac{R}{R}V_{in} + \left(1+\frac{R}{R}\right)V_{in}$$

$$\Rightarrow \quad V_{out} = -V_{in} + 2\,V_{in}$$

$$= -5\text{ V} + 10\text{ V}$$

$$= 5\text{ V}$$

9. (b)

$$\text{CMRR} = \frac{A_d}{A_c}$$

Given $\text{CMRR} = 40\text{ dB}$

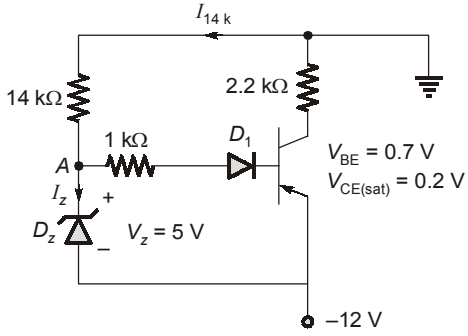
$$40 = 20\log_{10}\left(\frac{A_d}{A_c}\right)$$

$$\frac{A_d}{A_c} = 100$$

$$\text{CMRR} = 100$$

$$\therefore \quad A_c = \frac{2000}{100} = 20$$

11. (d)



$$I_{14\,k\Omega} = \frac{0 - V_A}{14\,k\Omega}$$

$$V_A = 5 - 12 = -7 \text{ V}$$

$$I_{14\,k\Omega} = \frac{7}{14} \text{ mA} = 0.5 \text{ mA}$$

because of the diode D_1 the transistor will not conduct, there will be no current in the base terminal of the transistor.

thus $$I_{14\,k\Omega} = I_z = 0.50 \text{ mA}$$

12. (b)

The circuit shown in the figure is of a voltage doubler circuit

(where V_L is the r.m.s voltage at the secondary side of the transformer).

$$\frac{V_{in}}{V_L} = \frac{N_1}{N_2}$$

$$V_L = V_{in}\left(\frac{N_2}{N_1}\right) = 120 \times \frac{1}{10} = 12 \text{ V}$$

$$\therefore \quad V_{L\,peak} = \sqrt{2} \times 12 \text{ V}$$

$$= 16.97 \text{ V}$$

$$V_{out} = 2 \times 16.97 \text{ V} \qquad \because \text{the given circuit is a voltage double.}$$

$$= 33.94 \text{ V}$$

13. (d)

$$V_{bias} = \frac{1 \times 10^3}{(1+6.8) \times 10^3} \times 15$$

$$= \frac{15}{7.8} = 1.92 \text{ V}$$

thus the diode will never conduct and $V_{out} = V_{in}$

thus the D.C. value of output is equal to 0 V.

14. (c)

$$R = 10 \text{ k}\Omega$$

$$C = 22 \text{ nF}$$

$$\tau = 1.1 \text{ RC}$$

$$= (1.1) \times 10\,(22)\,\mu\text{sec}$$

$$= 242\,\mu\text{sec}$$

15. (a)

$$\% \text{ load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{22 - 21}{21} \times 100$$

$$= 4.76\%$$

16. (b)

Given

$$V_{out} = 15\ V$$
$$R_1 = 240\ \Omega$$
$$R_2 = (0 \text{ to } 5)\ k\Omega$$

$$\left(\frac{R_1}{R_1+R_2}\right)15 = 1.25$$

$$1+\frac{R_2}{R_1} = \frac{15}{1.25}$$

$$\frac{R_2}{R_1} = 11$$

$$R_2 = 240 \times 11$$
$$R_2 = 2640\ \Omega$$
$$= 2.64\ k\Omega$$

17. (a)

$$V_{CC} = 20\ V$$
$$R_C = 1.5\ k\Omega$$
$$I_C = 5\ mA$$
$$V_{CE} = V_{CC} - I_C R_C$$
$$= 20 - (5 \times 10^{-3})\,(1.5 \times 10^3)$$
$$= 20 - 7.5$$
$$= 12.5\ V$$

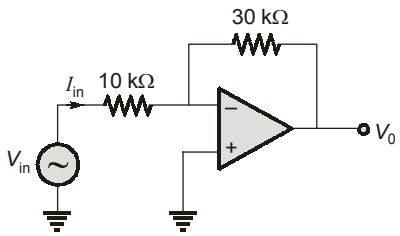
18. (b)

$$V_{GS} = 5\ V$$
$$V_{DD} = 30\ V$$

in saturation :

$$I_D = k_n(V_{GS} - V_T)^2$$
$$= 1 \times 10^{-3}\,(5-1)^2$$
$$= 16\ mA$$

20. (a)



$$I_{in} = \frac{V_{in}}{R_1}$$

$\Rightarrow$ $$\frac{V_{in}}{I_{in}} = R_1$$

$\therefore$ $$R_1 = R_{in} = \frac{V_{in}}{I_{in}} = 10\ k\Omega$$

22. (c)

$$\frac{5b+4}{4} = b+3$$

$$5b+4 = 4b+12$$

$$b = 8$$

23. (b)

$\because$ minimum base $\quad b_{min} = C + 1 = 13$

$\therefore \quad (11\,C)_{13} = 13^2 + 13 + 12$

$= 194$

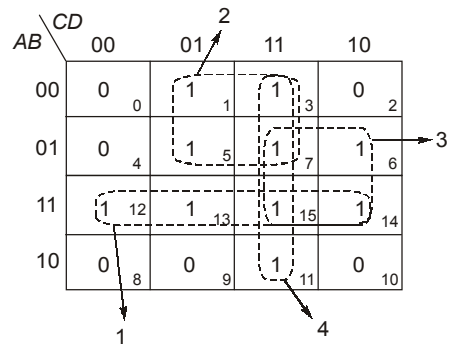
24. (b)

15's compliment is equivalent to $(r-1)$'s compliment

thus,

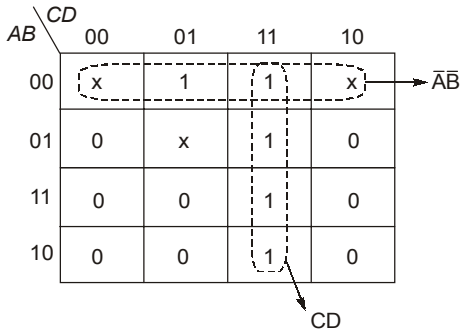
$$\begin{array}{r} F\ \ F\ \ F \\ -B\ \ B\ \ C \\ \hline (4\ \ 4\ \ 3)_{16} \end{array}$$

27. (a)



From the K-map it is clear that we have four essential prime implicants.

28. (c)



$$Y = CD + \bar{A}\bar{B}$$

30. (c)

As $Y = 1$ each bit will be complimented.

31. (a)

The excitation table of J K flip flop is as follows

Q_n	Q_{n+1}	J_n	K_n
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

33. (b)

$$\text{MOD } 78 = \text{MOD}(13) \times \text{MOD}(6)$$

34. (a)

$$T_p = \frac{1}{f_p} = 1\,\mu s$$

$$n = \text{number of FFs} = 10$$

Let t_{pd} = proagation delay of each FF

$$nt_{pd} \le T_p$$
$$t_{pd} \le 0.1\,\mu s$$
$$\le 100\,ns$$

35. (b)

$$Y = \bar{A} + A\bar{B} + A\bar{B}C$$
$$= \bar{A} + A\bar{B}$$
$$= \bar{A} + \bar{B}$$
$$= \overline{AB}$$

36. (d)

By using Bootstraping we can increase the small signal input resistance of the transistor.

37. (a)

For voltage amplification, we use cascaded structure of CE - CE.

38 (c)

The output will be same as the carry output of the full adder circuit. Thus the *K*-map of the output can be constructed as

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$Y = AB + BC + CA$$

Hence, maximum number of two input terms is = 3.

39. (c)

We use RTD and diodes to compensate the variation of transistors parameters with temperature while biasing a BJT.

40. (d)

For thermal runaway

Heat generated at the junction > Heat dissipated from the junction.

41. (d)

In the active region the base-collector junction is reverse biased. Thus the capacitance so formed is because of the base-collector transition region.

42. (b)

We use a negative feedback of voltage-shunt topologies to reduce the non-idealities which occurs in a transresistance amplifier.

43. (a)

The gain decreases, 3-dB frequency increases, noise figure increases and input impedance can increase or decrease based on the topology.

45. (c)

$$\text{Duty cycle} = \frac{T_{on}}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

$$= \frac{6}{10} = 0.6$$

46. (d)

Since it is a synchronous counter all the total time delay will be 25 ns.

48. (c)

The width of the pulse depend upon the timing circuit attached externally to the circuit which is made up of capacitors and resistors.

51. (a)

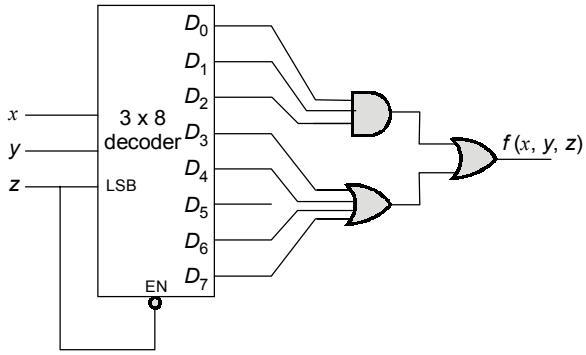
A charge couple device have sequentially accessed memory.

52. (c)

$$f_1 = \Pi M(0, 2, 7, 12, 13, 14, 15) + \Sigma d(6, 8)$$
$$f_1 = \Sigma m(1, 3, 4, 5, 9, 10, 11) + \Sigma d(6, 8)$$
$$f_2 = \Sigma m(0, 2,4, 7, 8, 15) + \Sigma d(6, 8)$$
$$f = f_1 \cdot f_2 = \Sigma\, m(4) + \Sigma d(6, 8)$$

53. (c)

The given 3 × 8 decoder is a active low output type.The circuit can be redrawn as shown in the figure below



if z = 0 then EN = 1 (thus we will get output only for even values)

The outputs D_0, D_2, D_4 and D_6 are active and outputs D_1, D_3, D_5 and D_7 are inactive

$\therefore$ output of OR gate is (D_3, D_4, D_6, D_7). But D_3 and D_7 will remain inactive.

output of AND gate is zero because all three inputs D_0, D_1 and D_2 can never be 1 at the same time.

$$f(x, y, z) = \Sigma m(4, 6)$$

54. (a)

Since loading is synchronous type, for every nibble to load one clock pulse is needed.

Number of Clock Pulses	Operation
1	LSB nibble written
4	LSB nibble read
1	MSB nibble written
4	MSB nibble read

$$\text{Total clock pulses} = 1 + 4 + 1 + 4$$
$$= 10$$

55. (a)

$$E = \overline{z}$$
$$S_1 = \overline{y}$$
$$S_0 = z$$
$$F = E\left[\overline{S}_1\overline{S}_0 I_0 + \overline{S}_1 S_0 I_1 + S_1\overline{S}_0 I_2 + S_1 S_0 I_3\right]$$
$$= \overline{z}\left[y\overline{z}x + yzx + \overline{y}\,\overline{z}\,y + \overline{y}\,z\,\overline{y}\right]$$
$$= xy\overline{z}$$

56. (d)

Register-A and Register-B together form a cyclic register.

So, contents in Register-A reappears after 7-clock pulses.

Clock Pulse	Register - A	Register - B
7	1 0 1 0	1 0 1
8	1 1 0 1	0 1 0
9	0 1 1 0	1 0 1
10	1 0 1 1	0 1 0

57. (a)

$$\Rightarrow \quad I_{L(max)} = \left(\frac{25-9}{10\ k}\right) - i_{z(min)} = 1.6 - 0.6 = 1\ mA$$

58. (c)

$$D = 1 + A\beta \qquad \text{(where, } D \text{ is the desensitvity factor)}$$

now, $$\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{99+1} = \frac{1}{100} = 0.01$$

$$\therefore \quad \%\text{ decrease in closed loop gain} = \frac{20\%}{1+5\times10^{3}\times10^{-2}} = \frac{20}{51}\%$$

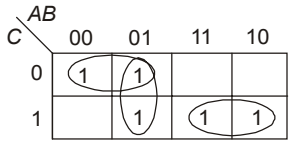
$$= 0.39\%$$

59. (a)

$$F = (A+B)(A+\bar{A}+\bar{B})C + \bar{A}(B+\bar{C}) + \bar{A}B + ABC$$

$$= AC + BC + \bar{A}B + \bar{A}\bar{C} + \bar{A}B + ABC$$

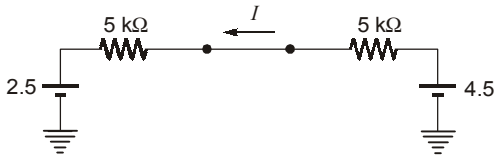
$$= AC + BC + \bar{A}(B+\bar{C})$$



using *K*-map $$F = AC + \bar{A}B + \bar{A}\bar{C}$$

60. (c)

Drawing the Thevenin equivalent of the above circuit and considering the diode to be short circuit, we have



$$\therefore \quad I = \frac{2\ V}{10\,k\Omega} = 0.2\ mA$$

61. (c)

Transmission Gate is a digitally controlled CMOS switch.

62. (c)

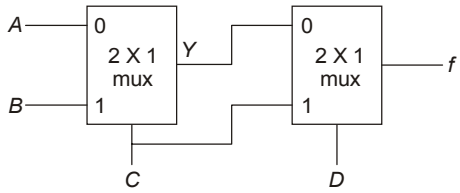
squaring both side, $(\sqrt{41})^2 = (5)^2$

$(41)_B = (25)_{10}$

$(4B+1)_{10} = (25)_{10}$

$\Rightarrow \quad B = 6$

63. (c)



$Y = A\bar{C} + BC$

$f = Y\bar{D} + CD$

$f = (A\bar{C} + BC)\bar{D} + CD = A\bar{C}\bar{D} + BC\bar{D} + CD$

$f(A,B,C,D) = \Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$

AB \ CD	00	01	11	10
00	0	1	1 (3)	2
01	4	5	1 (7)	1 (6)
11	1 (12)	13	1 (15)	1 (14)
10	1 (8)	9	1 (11)	10

64. (b)

$(0111111001)_2 - (0111110100)_2 = (101)_2 = (5)_{10}$

$\text{Resolution} = \dfrac{25\text{ mV}}{5} = 5\text{ mV}$

$\text{Full scale deflection} = \text{resolution} \times (2^n - 1)$

$= 5 \times 10^{-3} \times 1023 = 5.115 \text{ volts}$

65. (c)

$\because \quad A_1 = -2$

$\because \quad -\dfrac{R_2}{R_1} = -2$

$\Rightarrow$ for non inverting Amplifier gain

$A = \left(1 + \dfrac{R_2}{R_1}\right) = 3$

$\because \quad \dfrac{V_0}{V_2} = \dfrac{1}{2} \cdot (\text{gain})$ [Voltage divider circuit]

$= \dfrac{1}{2} \times 3 = \dfrac{3}{2} = 1.5$

67. (d)

The ripple factor of a half-wave ractifier is 1.21.

70. (c)

ECL dissipates more power than TTL.

72. (c)

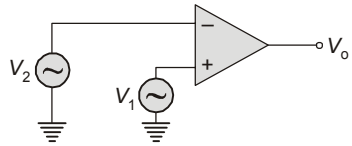
Only two NAND gates are not sufficient to accomplish any of the basic gate.

74. (d)

Thermal runaway occurs in BJT circuits only.

75. (c)

When an ideal op-amp is connected in amplifier mode, due to the concept of virtual short, both the inverting and non-inverting terminals of the op-amp should be at the same voltage i.e. both the input terminals are at the same potential.



$$\text{CMRR} = \frac{A_d}{A_{cm}} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

Common-mode gain is the gain when same inputs are applied at both the input terminals of Op-Amps

So $V_o = A_{cm}(V_1 - V_2)$

$\therefore$ $A_{cm} = 0$

$\therefore$ CMRR $\approx \infty$ (ideally) or very high practically

❍❍❍❍