OFFLINE TEST SERIES

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ESE-2017 : Prelims Exam

UPSC Engineering Services Examination

E & T ENGINEERING

Answer Key & Solutions

Test 15: Part Syllabus Technical

Advance Electronics + CO

1.	(c)	16.	(a)	31.	(a)	46.	(c)	61.	(d)
2.	(c)	17.	(c)	32.	(b)	47.	(a)	62.	(c)
3.	(a)	18.	(c)	33.	(d)	48.	(b)	63.	(c)
4.	(c)	19.	(d)	34.	(a)	49.	(b)	64.	(c)
5.	(c)	20.	(b)	35.	(b)	50.	(b)	65.	(b)
6.	(a)	21.	(c)	36.	(c)	51.	(d)	66.	(b)
7.	(b)	22.	(c)	37.	(b)	52.	(b)	67.	(a)
8.	(c)	23.	(d)	38.	(a)	53.	(c)	68.	(a)
9.	(d)	24.	(b)	39.	(c)	54.	(a)	69.	(a)
10.	(a)	25.	(c)	40.	(a)	55.	(a)	70.	(a)
11.	(a)	26.	(a)	41.	(d)	56.	(b)	71.	(a)
12.	(b)	27.	(c)	42.	(c)	57.	(a)	72.	(a)
13.	(c)	28.	(c)	43.	(b)	58.	(b)	73.	(d)
14.	(d)	29.	(b)	44.	(c)	59.	(b)	74.	(a)
15.	(d)	30.	(d)	45.	(b)	60.	(c)	75.	(d)

DETAILED EXPLANATIONS

1. (c)

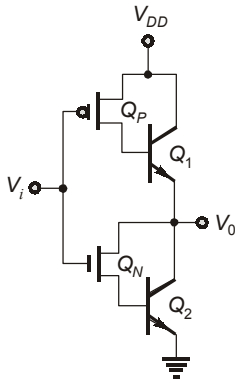
Ion-implantation is not a high temperature process.

2. (c)

The correct order of process steps used in photolithography is as follows:

Spinning
↓
Pre-bake
↓
Alignment and exposure
↓
Development
↓
Post-bake
↓
Oxide etching
↓
Photo-resist stripping

4. (c)



A basic Bi-CMOS inverter consists of two npn BJTs and one n-MOS and one p-MOS. So, option (c) is the correct choice among the given options.

17. (c)

CMOS fabrication	:	Latch-up
Ion implantation	:	Channeling
LOCOS	:	Bird's beak
Electron beam lithography	:	Proximity effect

18. (c)

Oxidation	:	Masking
Ion implantation	:	Doping
Metallization	:	Interconnecting
Photolithography	:	Patterning

28. (c)

The given state diagram is an example of serial adder.

29. (b)

The given state diagram is a sequence detector which detects the sequences 101 and 010.

31. (a)

Using state reduction,

PS	NS		O/P	
	$X=0$	$X=1$	$X=0$	$X=1$
a	a	b	0	0
b	c	a	1	1
c	d	a	1	1
d	d	a	1	1

$\Rightarrow d = c$

So, reduced state table after eliminating "d" can be given as

PS	NS		O/P	
	$X=0$	$X=1$	$X=0$	$X=1$
a	a	b	0	0
b	c	a	1	1
c	c	a	1	1

$\Rightarrow c = b$

Now, "c" also can be eliminated. So, the irredundant state table consists of "2" states.

So, $2^n \leq 2$; n = number of FFs required

$n \leq 1$

$n_{min} = 1$

33. (d)

When $A = 1$, Q will be selected by MUX and feedback to D flipflop which gives output Q again. So when $A = 1$ it holds its state.

When $A = 0$, $\bar{Q}$ will be selected by MUX and feedback to D flipflop and output will be inverted.

So for $A = 1$ it holds the state and for $A = 0$ it toggles the state.

So option (d) is correct.

35. (b)

Number of data lines required = 4 + 4 = 8

Number of address lines required = 4 + 4 = 8

So, ROM size = $2^8 \times 8$ = 256 Bytes

37. (b)

Disk capacity = Number of surface × number of tracks/surface × number of sector/track × sector size

= 250 × 272 × 190 × 40 B

= 516800000 B

38. (a)

$$\text{Number of disk block} = \frac{\text{Disk size}}{\text{Block size}}$$

$$= \frac{2\,GB}{128\,B} = \frac{2 \times 2^{30}}{2^7} = 2^{31-7}$$

$$= 2^{24} = 16\text{ M}$$

For each block one bit require so 16 Mbits are required.

Since memory is byte addressable. So, $= \frac{16\text{ M}}{8} = 2\text{ MB}$

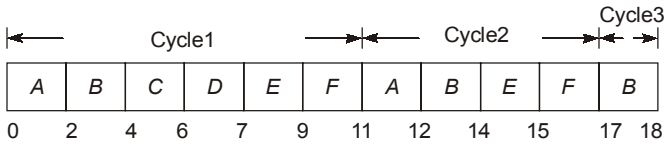
39. (c)

All threads share same address space and resources but maintains independent stack and thread control block for each thread of a process.

40. (a)

1. Thread running in critical section may get context switched, because 'locks' (user-level) are independent of the scheduler and if thread running in the Kernel with interrupts disabled would not get context switched.
2. Hardware access to devices is usually available in Kernal mode.
3. Modifications to the page tables are only possible in Kernel mode.

41. (d)



5 processes (*A*, *C*, *D*, *E*, *F*) have completed their execution.

42. (c)

Postfix expression evaluation take O(n) time because only one pass required for evaluation push element and pop 2 elements from stack, operate it and again push it onto stack whenever operator occurs.
Prefix and infix evaluation take $O(n^2)$ because two pass are require to evaluate.

43. (b)

To evaluate the infix and prefix expression 1 operator stack is used.
To evaluate the postfix expression 1 operand stack is used.

44. (c)

If the memory is allocated word by word then internal fragmentation can be avoided.
Segmentation can be used to avoid the internal fragmentation.
[**Note:** Paging suffers from internal fragmentation]

45. (b)

	After Execution			
main ( )	a	b	p	q
int a = 5, b = 6;	5	6		
int *p = &a, **q;	5	6	&a	–
*p = 20; q = &p;	20	6	&a	&p
f(a, &b);	20	20	&a	&p
*q = &b;	20	20	&b	&p
*p = 30;	20	30	&b	&p

a = 20, b = 30

46. (c)

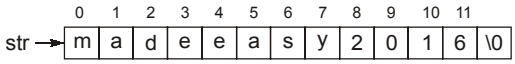
S_1: For better throughput larger block size used in fixed block size file system but it results decreases in the space utilization.

S_2: Number of DBA's possible in one disk block = $\frac{\text{DBA Size}}{\text{DBA}}$.

47. (a)

Every student can enroll more than one course.
Every course can be enrolled by more than one student.
Therefore it's many to many relationship.

48. (b)



Inside run( ). Pointer str2 is initialized as str1 and str1 is moved till '\0' is reached.
So str1 will increment by 12 then 12 – 0 = 12 will return.

49. (b)

Trace of matricx take a matrix $m = n = 3$

$$\begin{bmatrix} a & 0 & 0 \\ 0 & b & 0 \\ 0 & 0 & c \end{bmatrix}$$

then sum = 0 + a, sum = $a + b$, sum = $a + b + c$
sum = $a + b + c$
which is trace of matrix.

50. (b)

CSMA/CD do not prevent collisions but it ensures that ethernet works well even though collisions may occur.
After the jamming is complete, each sender randomizes a timer and waits that long before trying to resend the collided frame. All systems do not jam the network, only those involved in the collision. All do not begin transmitting again they wait a random amount of time.

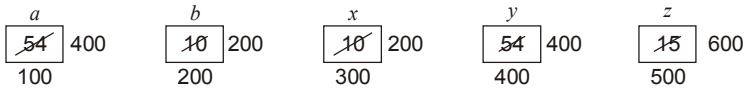
51. (d)

Short-term scheduler executes frequently to dispatch the process from the ready queue to CPU.
So, option (d) is correct and remaining options are the job of long term scheduler.

52. (b)

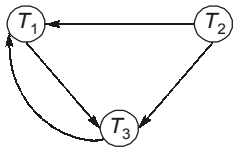
$$a = 20 + \text{Rec}(3) * \text{Rec}(4)$$
$$a = 20 + a + a \times a \times a + 1 + a + 1 \times a + 1$$
$$a = 20 + 3 + 3 \times 3 \times 3 + 1 + 3 + 1 \times 3 + 1$$
$$= 20 + 3 + 27 + 1 + 3 + 3 + 1$$
$$= 58$$

53. (c)



1. $x = x * (y + z)$;
   $x = x * (5 + 15)$
   $= 10 * (20) = 200$
2. $y = 200 << 1$
   $= (11001000)_2 << 1$
   $= (110010000)_2 = 400$
3. $z = x + y$
   $= 200 + 400 = 600$

54. (a)



Clearly we can see the cycle in precedence graph.
Therefore this schedule *S* is not conflict equivalent to any serial schedule.

55. (a)

p = 2
q = 3
*(A[0] + 0) = A[0] [0] = *(*(A + j) + i) = 1
*(A[1] + 0) = A[1] [0] = 2
Similarly it will access all the elements.
∴ 1 2 3 4 5 6 is the output printed by the program.

56. (b)

The given expression is: $(a - b) \uparrow (p + q) \uparrow (r * s * t)$

$= (ab-) \uparrow (pq+) \uparrow ((rs*) * t)$

$= (ab-) \uparrow (pq+) \uparrow ((rs*)*t)$

$= (ab-) \uparrow (pq + rs*t*) \uparrow$

$= (ab - pq + rs* t*) \uparrow\uparrow$

$= ab - pq + rs * t * \uparrow\uparrow$

57. (a)

Initial values i = –3, j = 2, k = 0.

&& has more priority than ++

$\therefore$ m = {(++i) && (++j)} || (++k);

Since both ++i and ++j are non-zero hence expression becomes true.

++k is not checked and m = truth value of expression = 1.

So, i = –2, j = 3, k = 0, m = 1.

58. (b)

No unlock operation can precede a lock operation in the same transaction.

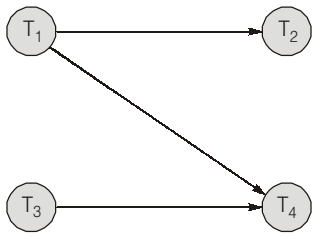
59. (b)

In S_2: $w_3(b)$ is first and $r_2(b)$ appears second

Hence, c_2 should appear after c_3.

In recoverable [If T_j is reads a value written by T_j, the Ti must commit after T_j commits]

60. (c)



After T_1, T_2 and T_4 should schedule

$\therefore$ T_1, T_4, T_3, T_2 is correct.

61. (d)

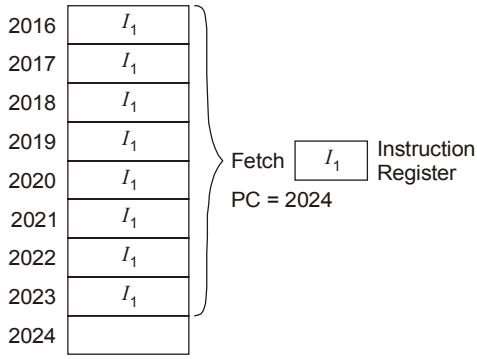
1	2	3	4	5	6	7	8	9	10	11	12	13	14
IF	ID	EX	MA	WB									
	IF	ID	EX	MA	WB								
		IF	ID	S	S	S	EX	MA	WB				
			IF	ID	S	S	S	S	S	S	EX	MA	WB

S = Stall

14 cycles are required.

62. (c)

8 byte instruction storage:



Effective address = PC + Relative value
= 2024 + (–11)
= 2013

63. (c)

$$\text{Speedup (S)} = \frac{1}{(1-\text{Cache \% used}) + \left[\frac{\text{Cache \% used}}{\text{Speedup using cache}}\right]}$$

$$= \frac{1}{(1-F)+\left(\frac{F}{S}\right)} = \frac{1}{(1-0.8)+\left(\frac{0.8}{20}\right)} = \frac{1}{(0.2)+\left(\frac{0.8}{20}\right)}$$

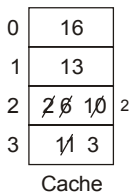
$$= \frac{1}{(0.2)+(0.04)} = \frac{1}{(0.24)}$$

$$= [0.24]^{-1} = 4.166$$

64. (c)

Cache data size = 16 words
Block size = 4 words

$$\text{Number of cache block} = \frac{16}{4} = 4$$



2% 4 = 2 ×
13% 4 = 1 ×
6% 4 = 2 ×
16% 4 = 0 ×
11% 4 = 3 ×
3% 4 = 3 ×
10% 4 = 2 ×
2% 4 = 1 ×
13% 4 = 1 ✓

Total # misses = 8 misses

65. (b)

$$\text{Biased exponent} = 18 + 64 = 82$$

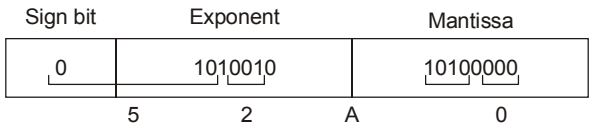
Representing 82 in binary

$$(82)_2 = (1010010)_2$$

Representing mantissa in binary

$$(0.625)_{10} = (0.10100000)$$

Floating point representation is as follows:



66. (b)

Both the statements are individually correct. Infact both are one and the same statement. But this is not the reason. In order to maintain integrity and consistency of the database, atomic property need to be satisfied.

73. (d)

SiO_2 also can be deposited on Si using CVD. If silane gas and oxygen are allowed to react above a silicon substrate, then the end product will be silicon dioxide deposited as a solid film on the silicon wafer surface.

75. (d)

The number of states in a Moore machine and in its equivalent Mealy machine are not always same.

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