ESE Main Examination

Electronics & Telecom. Engineering : Paper-I

(Previous Years Solved Paper 1999)

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MADE EASY PUBLICATIONS

1 Basic Electronics Engineering (EDC)

Revised Syllabus of ESE: *Basics of semiconductors; Diode/Transistor basics and characteristics; Diodes for different uses; Junction and Field Effect Transistors (BJTs, JFETs, MOSFETs); Optical sources/detectors; Basics of Opto electronics and its applications.*

6. Power Switching Devices

6.1 The electrical symbol representation of a four layer pnpn diode is shown below in the figure (a) and its VI characteristic is shown below in the figure (b).

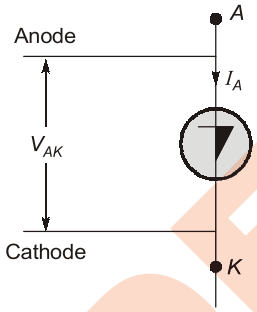


Fig. (a)

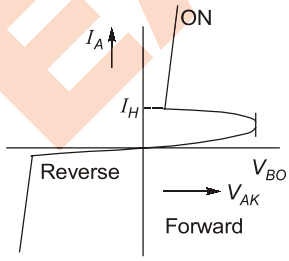


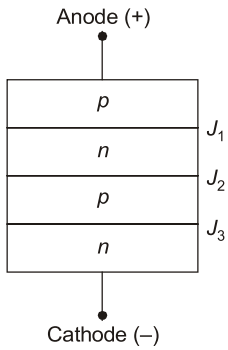
Fig. (b)

(a) Explain why the VI characteristic of the pnpn diode behaves as represented in figure (b).

(b) Can the above device be used as an electronic switch? If so why? [15 marks : 1999]

Solution:

(a) Four-layer p-n-p-n diode is shown in the figure given here.



⇒ When the voltage is applied in the reverse direction, the two outer junctions of the switch are reverse-biased. At an adequately large voltage, breakdown will occur at these junctions, as indicated, at the 'reverse avalanche' voltage V_{RA}.

⇒ When a forward voltage is applied, only a small forward current will flow until the voltage attains the breakover voltage V_{BO}. The corresponding current is I_{BO}. If the voltage V is increased beyond V_{BO}, the diode will switch from its OFF (blocked) state to its ON (saturation) state and will operate in the saturation region. The device is then said to latch. If the voltage is now reduced, the switch will remain ON until the current has decreased to I_H. This current is called the holding or latching current. The corresponding voltage V_H is called holding or latching voltage. The current I_H is the minimum current required to hold the switch in its ON state.

(b) The p-n-p-n diode when biased with the anode positive, has two states. One is very high resistance state, typically of the order of 100 M, and the other a very low resistance state, typically less than 10 Ω. When reverse-biased, this device acts like a typical p-n diode, having a very low leakage current.

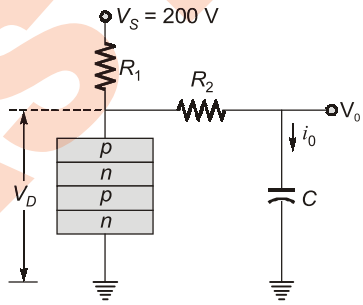
⇒ When an external voltage is applied to make the anode positive with respect to the cathode, junctions J_1 and J_3 are forward-biased and the centre junction J_2 is reverse-biased. The externally impressed voltage appears principally across the reverse-biased junction, and the current which flows through the device is small. As the impressed voltage is increased, the current increases slowly until a voltage called the firing, or breakover, voltage V_{BO} is reached where the current increases abruptly and the voltage across the device decreases sharply. At this breakover point the p-n-p-n diode switches from its OFF state to its ON state.

6.2 **Use the device to design a simple circuit to generate a continuous sawtooth wave of amplitude 100 volts, and repetitive frequency of 500 Hz. The following data is available regarding the four layer diode: V_{BO} = 100 V, I_A = 20 A, I_H = 20 mA.**

[25 marks : 1999]

Solution:

The circuit to generate a continuous sawtooth wave using a four layer *p-n-p-n* diode is shown here.



When the diode is OFF, it is effectively open and capacitor C charges to 200 V through R_1 & R_2. When $V_D = V_0$ reaches V_{BO} (= 100 V), the diode turns ON and acts like a (say 1 V = V_H) battery. The capacitor now discharges to V_H through R_2. When $i_D = i_0$ reaches the holding current I_H = 20 mA, the diode switches off and C begins to charge again also, I_A = 20 A.

When diode is ON:

$$V_0 = V_\infty - (V_\infty - V_1)e^{-t/T_{ON}}$$

where $V_\infty = 1$ V and $V_1 = 100$ V

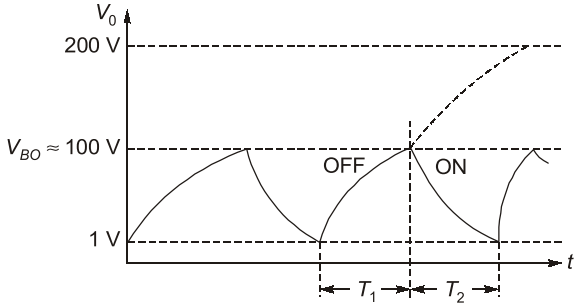
$$\therefore \quad V_0 = 1 + 99e^{-t/T_{ON}} \qquad \text{...(i)}$$

where $T_{ON} = R_2C$

Now, $$i_0 = C\frac{dV_0}{dt}$$

$$\Rightarrow \quad i_0 = \frac{-99}{T_{ON}}e^{-t/T_{ON}}$$

At $t = T_2$, $i_0 = -20 \times 10^{-3}$ A (Given)



When diode is OFF:

$$V_0 = V_\infty - (V_\infty - V_1)e^{-t/T_{OFF}}$$

where $V_\infty = 200$ V and $V_1 = 1.1$ V

$T_{OFF} = (R_1 + R_2)C \approx RC$

At $t = T_1$, $V_0 = 100$ V

$\because$ Repetitive frequency $= f = \dfrac{1}{T_1 + T_2} = 500$ Hz

After solving all the above equations we get,

R_1 = 1 MΩ, R_2 = 100 Ω and C = 5 μF.

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2 Materials Science

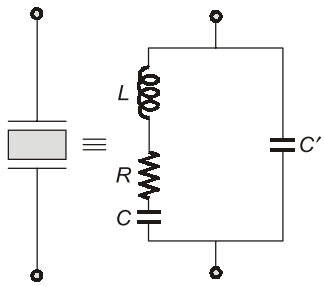
Revised Syllabus of ESE: *Electrical Engineering materials; Crystal structure & defects; Ceramic materials-structures, composites, processing and uses; Insulating laminates for electronics, structures, properties and uses; Magnetic materials, basics, classification, ferrites, ferro/para-magnetic materials and components; Nano materials-basics, preparation, purification, sintering, nano particles and uses; Nano-optical/magnetic/electronic materials and uses; Superconductivity, uses.*

2. Dielectric and Ceramic Materials

2.1 Draw the electrical equivalent circuit of a Quartz Crystal explaining the significance of the various components of the circuit. [10 marks : 1999]

Solution:

The electrical equivalent circuit of a quartz crystal is shown here.



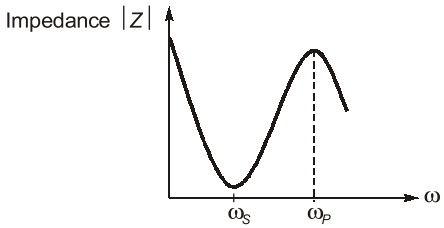
⇒ The inductor L, capacitor C and resistor R are the analogous to the mass, the compliance (the reciprocal of the spring constant) and the viscous-damping factor of the mechanical system. The shunt capacitance C' represents the electrostatic capacitance between electrodes with the crystal as a dielectric and its magnitude is very much larger than C. Because the crystal losses, represented by R, are small, **the equivalent quality factor of the crystal is high-typically 20,000.**

⇒ This Quartz crystal can be used for the Radio frequency oscillation.

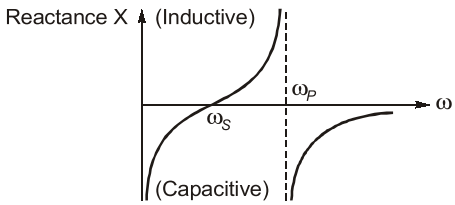
2.2 Draw neat sketches of Impedance versus Frequency, Reactance versus Frequency of the Quartz resonator indicating the critical frequencies and their values. [10 marks : 1999]

Solution:

- Crystal impedance versus frequency curve:



- Reactance versus frequency curve (if $R = 0$):



If we neglect the resistance R, the impedance of the crystal is a reactance jX whose dependence upon frequency is given by

$$jX = -\frac{j}{\omega C_P}\cdot\frac{\omega^2 - \omega_S^2}{\omega^2 - \omega_P^2}$$

where $\omega_S^2 = \frac{1}{L_s C_s}$ is the series resonant frequency (the zero impedance frequency), and $\omega_P^2 = \frac{1}{L_s}\left(\frac{1}{C_s} + \frac{1}{C_P}\right)$ is the parallel resonant frequency (the infinite impedance frequency).

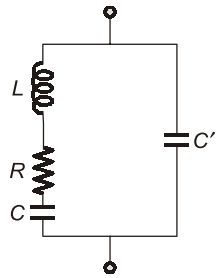
since $C_P >> C_s$, then $\omega_P \approx \omega_S$.

For $\omega_S < \omega < \omega_P$, the reactance is inductive and outside this range it is capacitive.

2.3 **A quartz crystal has the following electrical characteristics: Series resonance – 200 kHz Impedance at series resonance–200 ohms**
Parallel resonance at 200.25 kHz
Impedance at parallel resonance 40 MΩ
Determine the component values of the equivalent circuit. **[20 marks : 1999]**

Solution:

Consider an equivalent quartz crystal circuit as shown here,



Admittance of the equivalent circuit of the quartz crystal is

$$Y = \frac{1}{R + jX} + \frac{j}{X_{C'}} \quad ...(i)$$

where $X = X_L - X_C$

also $X_L = \omega L$

and $X_C = \frac{1}{\omega C}$

and $X_{C'} = \frac{1}{\omega C'}$

So, equation (i) may reduced to,

$$Y = \frac{R - jX}{R^2 + X^2} + \frac{j}{X_{C'}} = \frac{R}{R^2 + X^2} - j\left[\frac{X}{R^2 + X^2} - \frac{1}{X_{C'}}\right]$$

At resonance, imaginary part of the admittance will be zero, i.e.

$$\frac{X}{R^2 + X^2} = \frac{1}{X_{C'}}$$

or $(X^2 - X_{C'}) \cdot (X + R^2) = 0$ ...(ii)

Neglecting R,

$$X(X - X_{C'}) = 0$$

At series resonance, $X = 0 \Rightarrow X_L = X_C$

$$\Rightarrow \omega_S L = \frac{1}{\omega_S C}$$

$$\Rightarrow \omega_S = \frac{1}{\sqrt{LC}} \quad ...(iii)$$

At parallel resonance, $X - X_{C'} = 0 \Rightarrow X = X_{C'}$

$$\Rightarrow X_L - X_C - X_{C'} = 0$$

$$\Rightarrow \quad \omega_P L = \frac{1}{\omega_P C} + \frac{1}{\omega_P C'}$$

$$\Rightarrow \quad \omega_P^2 = \frac{1}{L}\left(\frac{1}{C} + \frac{1}{C'}\right)$$

$$\Rightarrow \quad \omega_P = \sqrt{\frac{1}{L}\left(\frac{1}{C} + \frac{1}{C'}\right)} \qquad \text{...(iv)}$$

At series resonance, $Y = \dfrac{R}{R^2 + X^2}$ and $X = 0$

so, $Y = \dfrac{1}{R}$

$\Rightarrow \quad Z = R = 200\ \Omega$

At parallel resonance, $X = X_{C'}$

$$Y = \frac{R}{R^2 + X_{C'}^2}$$

$$\Rightarrow \quad Z = \frac{R^2 + X_{C'}^2}{R} = 40 \times 10^6$$

$$\Rightarrow \quad 200 + \frac{X_{C'}^2}{200} = 40 \times 10^6$$

$$\Rightarrow \quad X_{C'} = 89442.495\ \Omega$$

$$\Rightarrow \quad \frac{1}{\omega_P C'} = 89442.495$$

$$\Rightarrow \quad C' = \frac{1}{2\pi \times 200.25 \times 10^3 \times 89442.495}$$

$$\Rightarrow \quad C' = 8.8859 \times 10^{-12}\ \text{F} = 8.8859\ \text{pF}$$

From equation (iv), $\omega_P^2 = \dfrac{1}{L}\left(\dfrac{1}{C} + \dfrac{1}{C'}\right) = \dfrac{1}{LC} + \dfrac{1}{LC'}$

$$\Rightarrow \quad \omega_P^2 = \omega_S^2 + \frac{1}{LC'} \qquad \text{[From eqn. (iii)]}$$

$$\Rightarrow \quad (2\pi \times 200.25 \times 10^3)^2 = (2\pi \times 200 \times 10^3)^2 + \frac{1}{L \times 8.8859 \times 10^{-12}}$$

$$\Rightarrow \quad L = 28.488\ \text{H}$$

Since, $\omega_S^2 = \dfrac{1}{LC}$

$$\Rightarrow \quad (2\pi \times 200 \times 10^3)^2 = \frac{1}{28.488\,C}$$

$$\Rightarrow \quad C = 0.02223\ \text{pF}$$

Thus, component values of the quartz crystals are as below:

$L = 28.488\ \text{H}$

$R = 200\ \Omega$

$C = 0.02223\ \text{pF}$

$C' = 8.8859\ \text{pF}$

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3 Electronic Measurements and Instrumentation

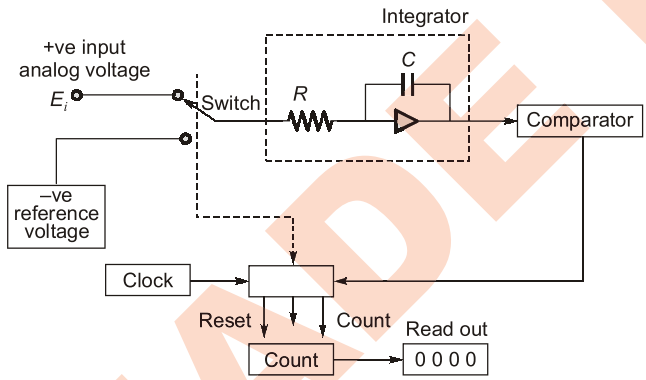
Revised Syllabus of ESE: *Principles of measurement, accuracy, precision and standards; Analog and Digital systems for measurement, measuring instruments for different applications; Static/dynamic characteristics of measurement systems, errors, statistical analysis and curve fitting; Measurement systems for non-electrical quantities; Basics of telemetry; Different types of transducers and displays; Data acquisition system basics.*

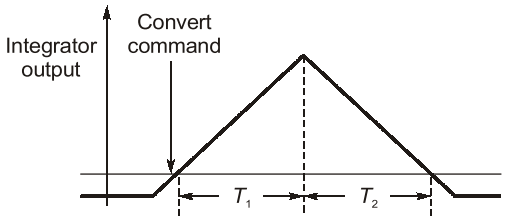
5. Digital System for Measurement

5.1 Explain the working of a Digital Voltmeter using the dual slope technique. [15 marks : 1999]

Solution:

Digital voltmeter using the dual slope technique:





⇒ The reference voltage and the input analog voltage are sequentially connected to the integrator with the help of a switch. The input voltage is integrated for a fixed input sample time. The integrated value is then discharged at a fixed rate and the time to do this is measured by a counter and finally displayed which indicates the value of voltage to be measured in digital form.

T_1 = Counts upto input voltage

T_2 = Counts upto reference voltage

Input voltage, $$E_i = \left(\frac{T_2}{T_1}\right) E_r$$

Where E_r is the reference voltage.

5.2 The DVM using the dual slope technique has a reference voltage of 1000 V and the fixed time 1000 counts. What is the voltage indicated if the counter reads 762 on the downwards slope?
[15 marks : 1999]

Solution:

Reference voltage, $E_r = 1000V$; Fixed time counts, $T_1 = 1000$
Counts read by counter, $T_2 = 762$

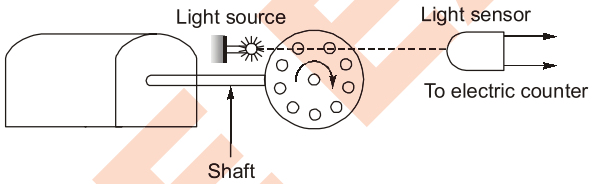
$$E_i = \left(\frac{T_2}{T_1}\right) E_r = \left(\frac{762}{1000}\right) 1000 = 762 \text{ V}$$

6. Transducers

6.1 The speed of a rotating shaft is to be measured by using a photo-electric device and an electronic counter. Sketch a suitable arrangement for making this measurement and comment on the accuracy of this method. [10 marks : 1999]

Solution:

- The arrangement to measure the speed of a rotating shaft using a photoelectric device and an electronic counter is called the photoelectric tachometer.
  Photoelectric tachometer : The arrangement is shown below:



⇒ The disc has a number of equidistant holes on its periphery. At one side of the disc a light source is fixed and at the other side of the disc, and on line with the light source, a light sensor such as a photo tube or photo sensitive semiconducting device is placed. When the opaque portion of the disc is between the light source and the light sensor, the latter is unilluminated and produces no output. But when a hole appears between the two, the light falling upon the sensor produces an output pulse.

⇒ The frequency at which these pulses are produced depends upon the number of holes in the disc and its speed of rotation. Since the number of holes is fixed, the pulse rate is a function of speed of rotation. The pulse rate can be measured by an electronic counter which can be directly calibrated in terms of speed in rpm.

⇒ The **accuracy** of this method depends principally on the error represented by one pulse. The digital meters measure frequency by counting the number of input pulses which occur in short period of time called gating period. If this period is too small, serious errors may be caused. The gating period should therefore, be chosen to give a sufficiently large count. In general, all the digits on the digital display should be utilized.

⇒ The factors which the user can control to minimize the errors are:

(i) gating period, and
(ii) number of pulses generated per revolution.

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4 Network Theory

Revised Syllabus of ESE: *Network graphs & matrices; Wye-Delta transformation; DC circuits-Ohm's & Kirchoff's laws, mesh and nodal analysis, circuit theorems; Linear constant coefficient differential equations- time domain analysis of RLC circuits; Solution of network equations using Laplace transforms- frequency domain analysis of RLC circuits; 2-port network parameters-driving point & transfer functions; State equations for networks; Single-phase AC circuits, Steady state sinusoidal analysis.*

3. Network Theorems

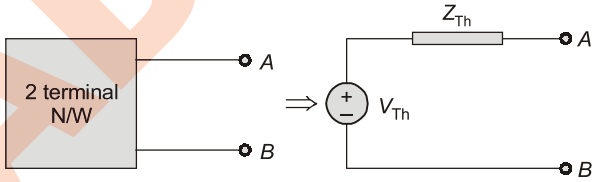
3.1 State clearly the Thevenin's and superposition theorems and explain their usefulness in linear network analysis.

[5 marks : 1999]

Solution:

■ Thevenin's Theorem:

- This theorem states that a linear, bilateral network consisting of active and passive elements can be replaced by a voltage source connected in series with an impedance. The value of voltage source is equal to the open-circuited voltage seen across the terminals and the impedance is equal to the impedance seen across the open-circuited terminals with all sources replaced by their internal impedances.



⇒ Usefulness of Thevenin's theorem in Linear Network

- Thevenin's theorem is very useful in linear network analysis because using Thevenin's theorem a large part of network, often a complicated and uninteresting part, can be replaced by a very simple equivalent which enables us to make rapid calculations.
- It is very useful when it is desired to determine the current through or voltage across any one element in a network instead of going through the lengthy method of solving the network.

■ Superposition Theorem:

- This theorem states that the voltage across or current through any element due to multiple sources present in a linear network is equal to the algebraic sum of voltage across or current through that element due to individual source with all other sources replaced by their internal impedances.

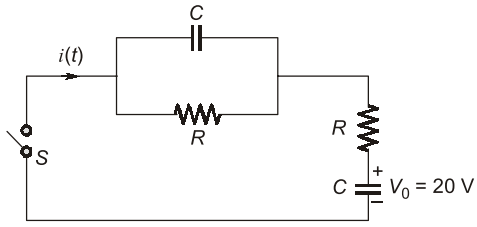
⇒ Useful of Superposition theorem:

- Superposition theorem is very useful in linear network analysis because a complex network can be solved easily by breaking it in simpler networks and using superposition theorem.

- This theorem is very useful to calculate the voltage and current when more than one active source is present in the network.
- Superposition is the combined property of homogeneity and additivity.

4. Transient State Analysis

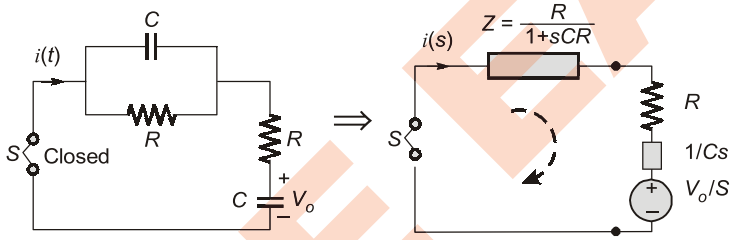
4.1 The circuit of the figure below is a well-known network used in control applications.



In the above figure $C = 1\ \mu F$, $R = 1\ M\Omega$ and the initial voltage V_0 across the right hand capacitor is 20 volts for $t < 0$ when the switch was open. At $t = 0$ the switch is closed. Determine (a) $i(t)$ after switch is closed. [25 marks : 1999]

Solution:

(a)



Applying KVL in s-domain,

$$\frac{R}{1+RCs}.I(s)+R.I(s)+\frac{1}{Cs}.I(s)+\frac{V_0}{s} = 0 \quad ; \quad \Rightarrow I(s).\left[\frac{R}{1+RCs}+R+\frac{1}{Cs}\right] = \frac{-V_0}{s}$$

$$\Rightarrow \quad I(s)\left[\frac{RCs+RCs(1+RCs)+(1+RCs)]}{Cs(1+RCs)}\right] = \frac{-V_0}{s}$$

$$\Rightarrow \quad I(s) = \frac{-V_0\,C\,(1+RCs)}{R^2C^2s^2+3\,RCs+1} \qquad \ldots(i)$$

Putting given numerical values we get,

$$I(s) = \frac{-20\times10^{-6}(1+s)}{s^2+3s+1} = \frac{-20\times10^{-6}(s+1)}{(s+2.62)\,(s+0.38)} \quad \text{[approximated factors]}$$

$$\Rightarrow \quad I(s) = -20\times10^{-6}\left[\frac{0.723}{s+2.62}+\frac{0.277}{s+0.38}\right] \qquad \ldots(ii)$$

Taking inverse Laplace transform of equation (ii) we get,

$$i(t) = -20\times10^{-6}[0.723\,e^{-2.62\,t}+0.277\,e^{-0.38\,t}]\ A$$

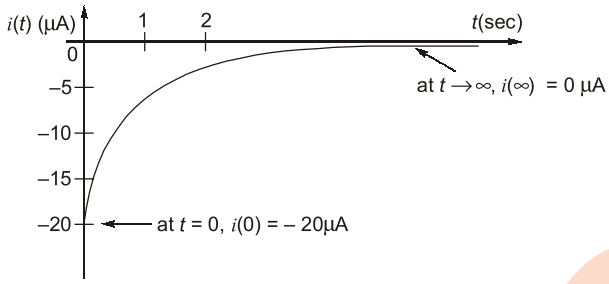
$$\Rightarrow \quad i(t) = -[14.46\,e^{-2.62\,t}+5.54\,e^{-0.38\,t}]\ \mu A \qquad \ldots(iii)$$

4.2 Plot $i(t)$ versus time on a graph paper indicating salient values. [10 marks : 1999]

Solution:

Plot of $i(t)$ versus time is shown below:

Here from equation (iii), (–)ve sign indicates that the plot is made down to the time axis.



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5 Analog Circuits

Revised Syllabus of ESE: *Small signal equivalent circuits of diodes, BJTS and FETs; Diode circuits for different uses; Biasing & stability of BJT & JFET amplifier circuits; Analysis/design of amplifier- single/multi-stage; Feedback& uses; Active filters, timers, multipliers, wave shaping, oscillators and other circuits; Basics of linear ICs, operational amplifiers and their applications-linear/non-linear.*

1. Diode Circuits

1.1 A power supply using half-wave rectifier is to have an output dc voltage of 30 V, with a load resistance of 500 Ω. The ripple factor should not exceed 0.01. Find a suitable value for *C*. Determine the peak diode current. Assume 50 Hz supply frequency. [8 marks : 1999]

Solution:

For Half-wave rectifier,

Ripple Factor $r = \dfrac{1}{2\sqrt{3}CR_L f}$

$$C = \frac{1}{2\sqrt{3}r R_L \times f} = \frac{1}{2\sqrt{3}\times 0.01\times 500\times 50} = 1.15 \text{ mF}$$

$$V_r = rV_{dc} = 0.01 \times 30 = 0.3 \text{ V}$$

$$V_r = \frac{I_{dc}}{Cf}$$

$$\Rightarrow \quad I_{dc} = fCV_r = 50 \times 1.15 \times 10^{-3} \times 0.3 = 0.01725 \text{ A}$$

2nd part: Peak diode current

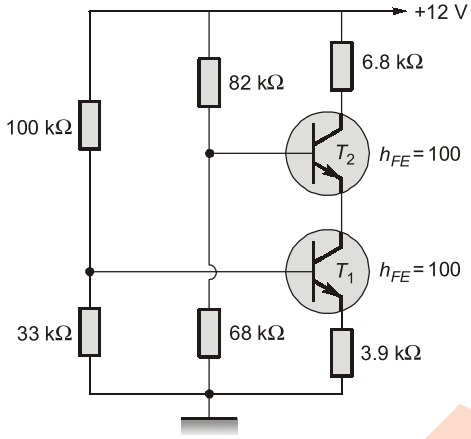
$$i_{D\max} = I_{dc}\left(1+2\pi\sqrt{\frac{2V_m}{V_r(p-p)}}\right)$$

$$\because \quad V_m \approx V_{dc}$$

$$i_{D\max} = 0.01725\left(1+2\pi\sqrt{\frac{2\times 30}{0.3}}\right) = 1.55 \text{ A}$$

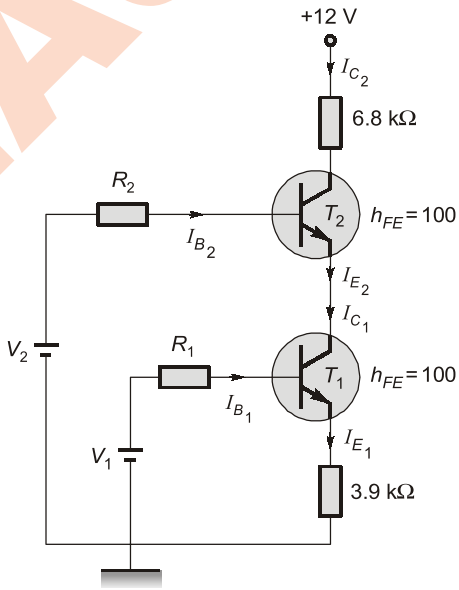
2. BJT Circuits

2.1 For the circuit shown below, calculate the Q point for both transistors. Assume silicon transistors, $V_{BE} = 0.7$ V. [8 marks : 1999]



Solution:

Rearranging the given circuit using Thevenin's equivalent,



Here, $$V_1 = \frac{33}{33+100} \times 12 = 2.977 \text{ V}$$

and $$R_1 = \frac{33 \times 100}{33+100} = 24.812 \text{ k}\Omega$$

and $$V_2 = \frac{68}{68+82} \times 12 = 5.44 \text{ V}$$

and $$R_2 = \frac{68 \times 82}{68+82} = 37.173 \text{ k}\Omega$$

Given: Applying KVL for transistor T_1,

$$V_{BE} = 0.7 \text{ V}$$

$$V_1 = R_1 I_{B_1} + V_{BE} + 3.9\, I_{E_1}$$

Putting, $$I_{B_1} = \frac{I_{C_1}}{h_{FE}}$$

and $$I_{E_1} = I_{C_1}\left(1 + \frac{1}{h_{FE}}\right)$$ and then substituting values,

$$\Rightarrow \quad 2.977 = 24.812 \frac{I_{C_1}}{100} + 0.7 + 3.9\left(1 + \frac{1}{100}\right) I_{C_1}$$

$$\Rightarrow \quad I_{C_1}(0.24812 + 3.9 \times 1.01) = 2.977 - 0.7$$

$$\Rightarrow \quad 4.18712\, I_{C_1} = 2.277$$

$$\Rightarrow \quad I_{C_1} = 0.5438 \text{ mA}$$

also, $$I_{E_2} = I_{C_1}$$

$$\therefore \quad I_{C_2} = \frac{I_{E_2}}{1 + \frac{1}{h_{FE}}} = \frac{I_{C_1}}{1 + \frac{1}{h_{FE}}} \Rightarrow I_{C_2} = \frac{0.5438}{1 + \frac{1}{100}} = \frac{0.5438}{1+0.01} = 0.5384 \text{ mA}$$

Applying KVL for Transistor T_2,

$$V_2 = R_2 I_{B_2} + V_{BE} + V_{CE_1} + 3.9\, I_{E_1}$$

Putting Values, $5.44 = 37.173\frac{I_{C_2}}{100} + 0.7 + V_{CE_1} + 3.9\left(1+\frac{1}{100}\right) I_{C_1}$

$\Rightarrow \quad 5.44 = 37.173 \times \frac{0.5384}{100} + 0.7 + V_{CE_1} + 3.9\left(1+\frac{1}{100}\right) I_{C_1}$

$\Rightarrow \quad V_{CE_1} = 2.3978\ \text{V}$

Now, $12 = 6.8\, I_{C_2} + V_{CE_2} + V_{CE_1} + 3.9\, I_{E_1}$

$\Rightarrow \quad 12 = 6.8 \times 0.5384 + V_{CE_2} + 2.3978 + 3.9 \times 1.01 \times 0.5438$

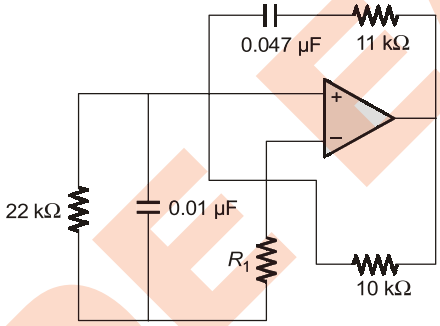
$\Rightarrow \quad V_{CE_2} = 3.799\ \text{V}$

So, Q-point for transistor T_1 is, $I_{C_1} = 0.5438\ \text{mA}$, $V_{CE_1} = 2.3978\ \text{V}$

and Q-point for transistor T_2 is, $I_{C_2} = 0.5384\ \text{mA}$, $V_{CE_2} = 3.799\ \text{V}$

6. Oscillators

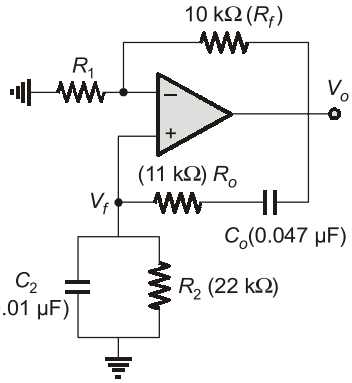
6.1 Determine the frequency of oscillation for the following circuit and the value of R_1 needed to maintain oscillations. Name the circuit.



[15 marks : 1999]

Solution:

The given circuit is a Wein Bridge oscillator. It can be redrawn as following:



$$\frac{V_f}{V_o} = \beta(s) = \frac{\left(R_2 \| \frac{1}{sC_2}\right)}{\left(R_2 \| \frac{1}{sC_2}\right) + \left(R_o + \frac{1}{sC_o}\right)} \quad \text{(Voltage division rule)}$$

$$\Rightarrow \beta(s) = \frac{\frac{R_2}{sC_2}}{\frac{R_2}{sC_2} + \left(R_2 + \frac{1}{sC_2}\right)\left(R_o + \frac{1}{sC_o}\right)} = \frac{sR_2C_o}{sR_2C_o + (sR_2C_2 + 1)(sR_oC_o + 1)}$$

$$\beta(s) = \frac{sR_2C_o}{s(R_2C_o + R_oC_o + R_2C_2) + s^2R_oC_oR_2C_2 + 1} \quad \ldots(i)$$

For $\beta(s)$ to be real $\left[\text{as } \left(1+\frac{R_f}{R_1}\right) \text{ is real}\right]$ for an oscillator

$$\Rightarrow \quad 1 + s^2 R_o C_o R_2 C_2 = 0 \quad \ldots(ii)$$

$$1 - \omega_o^2 R_o C_o R_2 C_2 = 0 \quad \Rightarrow \quad \boxed{\omega_o = \frac{1}{\sqrt{R_o C_o (R_2 C_2)}}}$$

$$\omega_o = \text{Frequency of oscillation} = \frac{1}{\sqrt{(0.517\times10^{-3})(0.22\times10^{-3})}}$$

$$\omega_o = \frac{1}{\sqrt{0.517\times0.22}}\times10^3 = 2.965\times10^3 \text{ radians/sec.} \Rightarrow \boxed{f_o = 471.915\,\text{Hz}}$$

Using equation (i) and (ii) $\beta(s)$ reduces to

$$\beta(s) = \frac{R_2 C_o}{R_2 C_o + R_o C_o + R_2 C_2}$$

Using Barkhausen criteria $A\beta = 1$

$$\Rightarrow \quad \left(1+\frac{R_f}{R_1}\right)\cdot\frac{R_2 C_o}{R_2 C_o + R_o C_o + R_2 C_2} = 1$$

$$\left(1+\frac{R_f}{R_1}\right) = \frac{R_2 C_o + R_o C_o + R_2 C_2}{R_2 C_o}$$

$$1+\frac{R_f}{R_1} = 1+\frac{R_o}{R_2}+\frac{C_2}{C_o}$$

$$\Rightarrow \quad \frac{R_f}{R_1} = \frac{R_o}{R_2}+\frac{C_2}{C_o} \qquad \text{...(iii)}$$

(iii) Equation is the most general condition for oscillation in the given Wein Bridge oscillator circuit. Putting the values of known components in (iii) equation we get,

$$\frac{10\text{k}}{R_1} = \frac{11\text{k}}{22\,\text{k}}+\frac{0.010\,\mu\text{F}}{0.047\,\mu\text{F}}$$

$$\Rightarrow \quad \frac{10\text{k}}{R_1} = 0.5 + 0.2127 \quad \Rightarrow \quad R_1 = \frac{10\,\text{k}}{0.7127}$$

$$\Rightarrow \quad R_1 = 14.029\,\text{k}\Omega$$

This is the value of R_1 for which the Wein Bridge oscillator will sustain oscillations.

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6 Digital Circuits

Revised Syllabus of ESE: *Boolean algebra & uses; Logic gates, Digital IC families, Combinatorial/sequential circuits; Basics of multiplexers, counters/registers/ memories, design & applications. MUX/ROM/PLA-based design, Moore & Mealy circuit design. A/D-D/A converters.*

4. Memories and Programmable Logic Devices

4.1 What is a ROM? Write the truth table of a 2-to-4 decoder with output polarity control and built with discrete gates and with an 8 × 4 ROM. [10 marks : 1999]

Solution:

ROM:

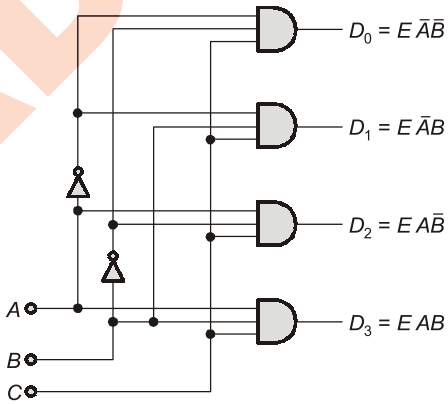
- Read-only memory is a type of semiconductor memory which stores information permanently.
- It is a non-volatile memory.
- It is a non-erasable memory (data once written cannot be erased).

Output polarity control refers to the 'enable input' (E) of the decoder.

Truth table of 2×4 decoder with output polarity control is shown,

E	A	B	D_0	D_1	D_2	D_3
1	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Logic gates diagram:

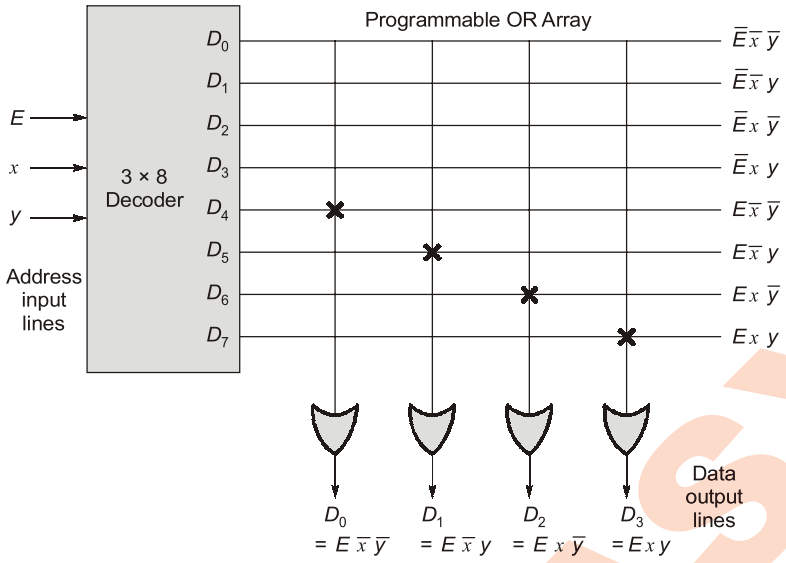


Implementation of 2 × 4 decoder using an 8 × 4 ROM

⇒ $2^3 \times 4$ ROM

⇒ (3×2^3 decoder) followed by (4 OR gates)

⇒ 3 address input lines and 4 data output lines

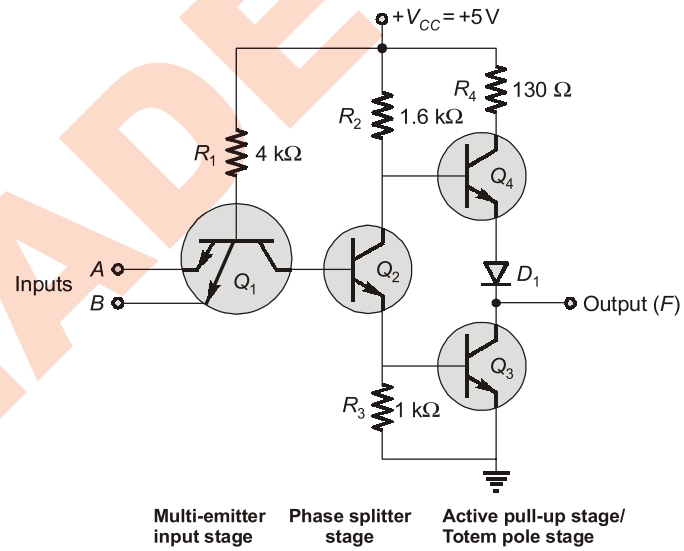


5. Logic Families

5.1 Draw the circuit diagram of a two input TTL NAND gate and label component values and write the function table. [3 + 3 marks : 1999]

Solution:

Two-input TTL NAND gate:



Function table:

- In this arrangement transistor (Q_1) is a multiple emitter transistor.
- Here diode (D_1) is connected to the output section in order to cutoff the 'Q_3' when transistor 'Q_4' is ON.

Inputs		Output
A	B	F
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

5.2 Define fan out. Which factor is responsible for the limit of fan out in TTL circuits? [4 marks : 1999]

Solution:

Fan out:

- The fan out is the maximum number of inputs that can be connected to the output of a gate, and is expressed by a number.
- In other words, the fan out or loading factor is defined as the maximum number of standard logic inputs that an output can drive reliably.

$\Rightarrow$ The fan out in TTL circuits is limited by the amount of current that the output transistor can sink in LOW state or can source in HIGH state.

5.3 "Loading an output with more than its rated fan out has several effects." – Write at least five effects. [6 marks : 1999]

Solution:

Loading an output with more than its rated fan out has the following effects:

(i) The device ceases to operate properly and is said to be overloaded.

(ii) Working of transistor is affected.

(iii) Rise time and fall time of the gates are affected.

(iv) Propagation delay of each gate is affected.

(v) Power dissipation in each gate is affected.

(vi) The transistors may get damaged.

(vii) The output logic-level voltages cannot be guaranteed.

(viii) Speed of operation gets affected.

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