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PTQ

Prelims Through Questions

for

ESE 2021

Electronics & Telecommunication

Day 5 of 11

Q.181 - Q.230

(Out of 500 Questions)

Basic Electronics Engineering + Analog Circuits

Basic Electronics Engineering + Analog Circuits

Q.181 A silicon diode is carrying a current of 1 mA. When the temperature of the diode is 20°C, diode voltage is found to be 700 mV. But the diode is operated at some other temperature where diode voltage is 600 mV. Then the new operating temperature of diode is

(a) 30°C (b) 40°C

(c) 50°C (d) 60°C

181. (d)

We know that,

Diode voltage V_D decreases by 2.5 mV per 1°C rise in temperature.

Given, temperature, $T_1 = 20°C$

$$\frac{\Delta V_D}{\Delta T} = -2.5 \text{ mV/°C}$$

$$\frac{V_{D2} - V_{D1}}{(T_2 - 20)} = -2.5 \times 10^{-3}$$

$$\therefore \quad \frac{(600-700)\times 10^{-3}}{-2.5\times 10^{-3}} = T_2 - 20$$

$$\therefore \quad T_2 = 60°C$$

Q.182 An abrupt p^+–n junction has depletion width of 4 μm and built-in potential at junction is 0.8 V. Assume another abrupt p-n^+ junction has depletion width of 8 μm, to maintain the same built-in potential as in the case of p^+-n junction, the required doping concentration is equal to (Assume, donor concentration $N_D = 4 \times 10^{16}$ cm^{-3})

(a) N_D (b) $2N_D$

(c) $\frac{N_D}{2}$ (d) $\frac{N_D}{4}$

182. (d)

Given, for p^+-n abrupt junction,

Depletion width, $W_1 = 4$ μm

Built-in potential, $V_{b1} = 0.8$ V

For another p-n^+ abrupt junction,

Depletion width, $W_2 = 8$ μm

Built-in potential, $V_{b2} = V_{b1} = 0.8$ V

Acceptor doping concentration, $N_A = ?$

We know that,

The depletion width,

$$W = \sqrt{\frac{2\varepsilon_s V_b}{q}\left[\frac{1}{N_A} + \frac{1}{N_D}\right]}$$

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For p^+-n abrupt junction, depletion width

$$W_1 = \sqrt{\frac{2\varepsilon_s}{q}\frac{1}{N_D}V_{b1}} \quad ...(i)$$

$\because$ for p^+-n junction, $N_A >> N_D$

For p-n^+ abrupt junction, depletion width

$$W_2 = \sqrt{\frac{2\varepsilon_s}{q}\frac{1}{N_A}V_{b2}} \quad ...(ii)$$

$\because$ for p-n^+ junction, $N_D >> N_A$

By dividing equation (i) with equation (ii),

$$\frac{W_1}{W_2} = \sqrt{\frac{N_A}{N_D}}$$

$$\frac{1}{2} = \sqrt{\frac{N_A}{N_D}}$$

$$\frac{1}{4} = \frac{N_A}{N_D}$$

$$\Rightarrow \quad N_A = \frac{N_D}{4} = 10^{16}\ \text{cm}^{-3}$$

Q.183 A MOSFET is operated in saturation region and channel length modulation is present. Then the drain to source conductance (g_{ds}) in terms of channel length modulation parameter (λ) is

(a) $g_{ds} = \dfrac{I_D}{1+\lambda V_{DS}}$ (b) $g_{ds} = \dfrac{I_D}{\frac{1}{\lambda}+V_{DS}}$

(c) $g_{ds} = \dfrac{I_D}{\frac{2}{\lambda}+V_{DS}}$ (d) $g_{ds} = \dfrac{2I_D}{\frac{1}{\lambda}+V_{DS}}$

183. (b)

Given, MOSFET is operated in saturation region and channel length modulation is present,

$\therefore$ Drain current, $$I_D = \mu_n C_{ox}\frac{W}{2L}(V_{GS}-V_T)^2\,[1+\lambda V_{DS}] \quad ...(i)$$

Drain to source conductance,

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox}\frac{W}{2L}(V_{GS}-V_T)^2\,(\lambda) \quad ...(ii)$$

From equation (i), we can write,

$$\frac{I_D}{1+\lambda V_{DS}} = \mu_n C_{ox}\frac{W}{2L}(V_{GS}-V_T)^2$$

We can re-write equation (ii) as,

$$g_{ds} = \frac{I_D}{1+\lambda V_{DS}}\cdot\lambda$$

or, $$g_{ds} = \frac{I_D}{\frac{1}{\lambda}+V_{DS}}$$

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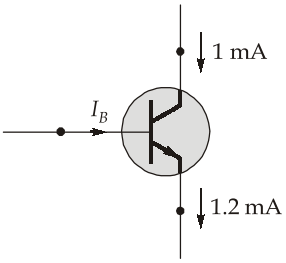
Q.184 A phosphorus doped silicon semiconductor (doping density : 10^{17} cm^{-3}) is heated from 100°C to 200°C. Which one of the following statements is correct?

(a) Position of fermi level moves towards conduction band
(b) Position of dopant level moves towards conduction band
(c) Position of fermi level moves towards middle of energy gap
(d) Position of dopant level moves towards middle of energy gap

184. (c)

Q.185 Consider the following transistor circuit shown below:



The BJT is operated in
(Assume $\beta_{min} = 50$)

(a) Active region
(b) Cut-off region
(c) Saturation region
(d) None of these

185. (c)

Given, Collector current, $I_C = 1$ mA
Since, $I_C = 1$ mA $> 0 \Rightarrow$ BJT not in cut-off region.
Emitter current $I_E = 1.2$ mA
But $I_E = I_B + I_C$
$\Rightarrow$ $I_B = I_E - I_C = 0.2$ mA

$$\beta = \frac{I_C}{I_B} = \frac{1\text{ mA}}{0.2\text{ mA}} = 5 < \beta_{min}$$

$\therefore$ BJT is in saturation region.

Q.186 Which of the following equation represents 'α' interms of I_C, I_B and I_{CO}?
(where, I_C = Collector current, I_B = Base current, I_{CO} = Reverse saturation current)

(a) $\frac{I_C + I_{CO}}{I_B + I_C}$
(b) $\frac{I_B + I_{CO}}{I_C - I_{CO}}$
(c) $\frac{I_C - I_{CO}}{I_B + I_C}$
(d) $\frac{I_B - I_{CO}}{I_B + I_{CO}}$

186. (c)

We know that,
Collector current, $I_C = \beta I_B + (1 + \beta) I_{CO}$
$I_C = \beta I_B + \beta I_{CO} + I_{CO}$

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$$\therefore \quad \beta = \frac{I_C - I_{CO}}{I_B + I_{CO}}$$

but, $$\alpha = \frac{\beta}{1+\beta} = \frac{\frac{I_C - I_{CO}}{I_B + I_{CO}}}{1 + \frac{I_C - I_{CO}}{I_B + I_{CO}}} = \frac{I_C - I_{CO}}{I_B + I_{CO} + I_C - I_{CO}}$$

$$\therefore \quad \alpha = \frac{I_C - I_{CO}}{I_C + I_B}$$

Q.187 An n-type silicon with doping carrier concentration $N_D = 10^{16}$ cm^{-3} is given. If this sample is uniformly illuminated, the steady state minority concentration in the sample will be 4×10^4 cm^{-3}. Then the rate at which electron-hole pairs (EHPs) are generated is
(Assume, intrinsic carrier concentration $n_i = 1.5 \times 10^{10}$ cm^{-3}, minority carrier life time $\tau_p = 10^{-6}$ sec)

(a) 1.00×10^{10} cm^{-3}/s (b) 1.25×10^{10} cm^{-3}/s
(c) 1.75×10^{10} cm^{-3}/s (d) 2.00×10^{10} cm^{-3}/s

187. (c)

We know that,

$$P = p_0 + G_L \tau_p$$

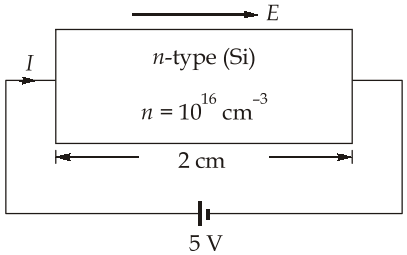
where,
P = Steady state minority concentration
p_0 = Thermal equilibrium concentration of holes
τ_p = Carrier life time
G_L = Generation rate of EHPs

but $$p_0 = \frac{n_i^2}{N_D} = \frac{(1.5\times10^{10})^2}{10^{16}} = 2.25\times10^4 \text{ cm}^{-3}$$

$$\therefore \quad G_L = \frac{P - p_0}{\tau_p} = \frac{(4\times10^4) - (2.25\times10^4)}{10^{-6}}$$

$$\therefore \quad G_L = 1.75 \times 10^{10} \text{ cm}^{-3}/\text{s}$$

Q.188 Consider a silicon semiconductor bar shown below:



The electron current density in the above semiconductor is
(Assume mobility of electron is 2500 cm^2/V-sec)

(a) 5 A/cm^2 (b) 10 A/cm^2
(c) 20 A/cm^2 (d) 25 A/cm^2

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188. **(b)**

From the given semiconductor bar,

$$\text{Electric field, } E = \frac{V}{l} = \frac{5}{2} = 2.5 \text{ V/cm}$$

Electron current density in the silicon bar,

$$J_n = nq\mu_n E$$
$$= 1.6 \times 10^{-19} \times 10^{16} \times 2500 \times 2.5$$
$$J_n = 10 \text{ A/cm}^2$$

Q.189 In a forward biased pn junction, the sequence of events that best describes the mechanism of current flow is

(a) injection, and subsequent diffusion and recombination of minority carriers
(b) injection, and subsequent drift and generation of minority carriers
(c) extraction, and subsequent diffusion and generation of minority carriers
(d) extraction, and subsequent drift and recombination of minority carriers

189. **(a)**

In a forward biased pn-junction diode, the current flow is due to diffusion of majority carriers and recombination of minority carriers.

Q.190 A semiconductor has a resistivity of 1.5 Ω-cm, and a Hall coefficient of –1250 cm^3/C. Then the mobility in the semiconductor is

(Assume only one type of charge carriers present and neglect random thermal distribution of speed).

(a) 655 $\text{cm}^2/\text{V-sec}$ (b) 750 $\text{cm}^2/\text{V-sec}$
(c) 833 $\text{cm}^2/\text{V-sec}$ (d) 910 $\text{cm}^2/\text{V-sec}$

190. **(c)**

Given, resistivity, $\rho = 1.5$ Ω-cm

Hall coefficient, $R_H = -1250 \text{ cm}^3/\text{C}$

Since, R_H is negative, the charge carriers are electrons.

Mobility, $\mu_e \approx \sigma |R_H|$

$$= \frac{1}{\rho}|R_H| = \frac{1}{1.5} \times 1250$$

$\therefore$ $= 833 \text{ cm}^2/\text{V-sec}$

Q.191 An ideal *n*-channel MOSFET has the following parameters, $\mu_n C_{ox} \frac{W}{L} = 1.5 \times 10^{-3} \text{ A/V}^2$, threshold voltage $V_T = 0.65$ V and oxide thickness is 0.4 nm. It is found that the MOSFET is operating in saturation region with $V_{DS} = 6$ V. Then the power dissipation in the MOSFET with $V_{GS} = 4$ V is

(a) 25.25 mW (b) 37.65 mW
(c) 50.50 mW (d) 75.50 mW

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191. **(c)**

Given, $\mu_n C_{ox}\frac{W}{L} = 1.5\times10^{-3}\ A/V^2$

$V_T = 0.65\ V$

$V_{GS} = 4\ V$

$V_{DS} = 6\ V$

Power dissipation in the MOSFET is,

$P = V_{DS} \times I_{DS}$

where, I_{DS} is drain to source saturation current.

Since the MOSFET is operating in saturation region,

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

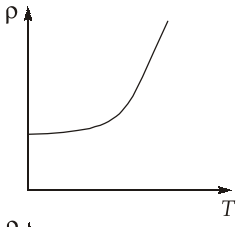
$$= \frac{1}{2}\times1.5\times10^{-3}(4-0.65)^2$$

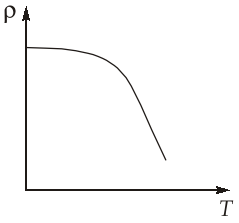
$I_{DS} = 8.42 \times 10^{-3}\ A$

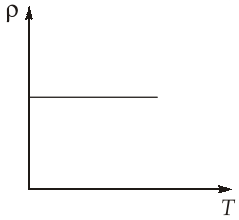
Power dissipation, $P = 6 \times 8.42 \times 10^{-3}$

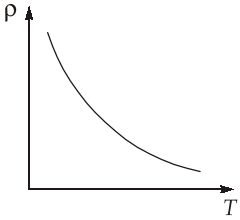
$\therefore$ $P = 50.50\ mW$

Q.192 Temperature dependence of resistivity of a metal can be described by

(a) 

(b) 

(c) 

(d) 

192. **(a)**

The conductors have the positive temperature coefficient of resistance. The conductors have almost linear increase in resistivity.

Q.193 Which of the following statement is NOT correct?

(a) MOSFETs are less noisy than BJTs.

(b) MOSFETs have lower power dissipation than BJTs.

(c) MOSFETs require lower area for the process of fabrication than BJTs.

(d) Switching speed of MOSFETs is higher than BJTs.

193. **(d)**

MOSFETs have less switching speed when compared to BJTs, because of oxide capacitance formation due to SiO_2 layer.

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Q.194 The semiconductor in a Hall experiment has magnetic field (B) = 0.5 Wb/m^2, width (W) = 0.1 m, current (I) = 10 mA and Hall coefficient (R_H) = 3.8 × 10^{-4} m^3/C. Then the type of the semiconductor and Hall voltage are respectively

(a) n-type and 1.9 μV (b) p-type and 1.9 μV
(c) n-type and 19 μV (d) p-type and 19 μV

194. (d)

Since, the given Hall coefficient is positive,

i.e., $R_H = 3.8 \times 10^{-4}$ m^3/C

The given semiconductor is p-type.

Hall voltage, $V_H = \dfrac{R_H BI}{W} = \dfrac{3.8\times10^{-4}\times0.5\times10\times10^{-3}}{0.1}$ V = 19 μV

Q.195 For a photodiode, the quantum efficiency is 80%. A monochromatic light having photon energy of 2 eV is incident on it, which produces the incident power of 10 mW. The generated photo current will be

(a) 2 mA (b) 2.5 mA
(c) 4 mA (d) 4.5 mA

195. (c)

Quantum efficiency, $\eta = \dfrac{I_L / q}{P_{in} / h\nu}$

I_L is in amperes
q is in Coulomb
P_{in} is in Watts
$h\nu$ is in Joules

$$h\nu = 2 \text{ eV} = 2 \times 1.6 \times 10^{-19} \text{ J} = 2q \text{ J}$$

$$\therefore \quad \eta = \frac{I_L}{P_{in} / 2} \quad \Rightarrow 0.8 = \frac{I_L}{\frac{10\times10^{-3}}{2}}$$

∴ Generated photo current,

$I_L = 4$ mA

Q.196 Consider the following statements regarding solar cell:

1. Fill factor is a measure of the realizable voltage from solar cell.
2. Typically, fill factor in a solar cell is between 0.7 and 0.8.
3. Maximum efficiency of a silicon pn junction solar cell is approximately 28%.

Which of the above statements is/are INCORRECT?

(a) 1 only (b) 2 and 3 only
(c) 1 and 2 only (d) 1, 2 and 3

196. (a)

Fill factor is a measure of the realizable power from solar cell.

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Q.197 Consider the following statements regarding "diffusion capacitance (C_D)" of a *pn* junction diode.

1. C_D is proportional to forward current I_f.
2. Under forward bias condition of *pn* junction, a large number of charge carriers are stored inside the depletion region which gives rise to C_D.
3. C_D is independent of temperature.

Which of the above statements is/are correct?

(a) 1 only (b) 1 and 2 only
(c) 2 and 3 only (d) 1, 2 and 3

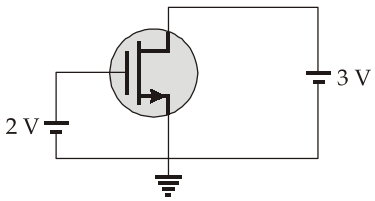
197. (a)

Diffusion capacitance, $C_D = \dfrac{\tau I_f}{\eta V_T}$

$C_D \propto I_f$; $C_D \propto \dfrac{1}{T}$

Under forward bias condition of *pn* junction, a large number of charge carriers are stored outside the depletion region, which gives rise to diffusion capacitance.

Q.198 An *n*-type MOSFET, with a threshold voltage of 1 V, is shown below. The region of operation of the MOSFET is



(a) Cut-off (b) Sub-threshold
(c) Linear (d) Saturation

198. (d)

$$V_{GS} - V_T = 2 - 1 = 1 \text{ V}$$
$$V_{DS} = +3 \text{ V} \quad \text{given}$$
$$\therefore \quad V_{DS} > V_{GS} - V_T$$
$\Rightarrow$ Saturation region

Q.199 For a JFET, $I_{DSS} = 20$ mA, $V_{GS(off)} = -5$ V and $g_{mo} = 4$ m℧. The transconductance of the JFET for $V_{GS} = -4$ V is

(a) 0.4 m℧ (b) 0.6 m℧
(c) 0.8 m℧ (d) 1 m℧

199. (c)

Transconductance of a JFET,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] = 4 \times 10^{-3}\left[1 - \frac{(-4)}{(-5)}\right] = 0.8 \text{ m℧}$$

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Q.200 Compared to a visible red LED, an infrared LED
(a) produces light with shorter wavelengths
(b) produces light of all wavelengths
(c) produces only one colour of light
(d) produces light with longer wavelengths

200. (d)

Q.201 In a particular *p-n* junction, with uniform doping profiles on the *p*-side and *n*-side, the peak electric field across the junction is 1.80×10^6 V/m and the width of the depletion region is 0.50 μm. If the junction is under thermal equilibrium condition, then the built-in potential of the junction will be
(a) 0.45 V (b) 0.60 V
(c) 0.90 V (d) 1.80 V

201. **(a)**

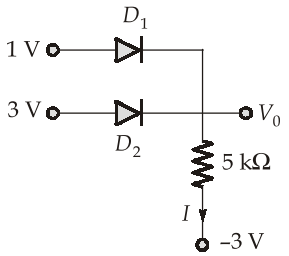
$$V_{bi} = \frac{1}{2} E_{max}\, x_{dep}$$
$$= \frac{1}{2} \times 1.80 \times 10^6 \times 0.50 \times 10^{-6} = \frac{1.80}{4} = 0.45 \text{ V}$$

Q.202 Consider the following statements regarding "Mass action law":
1. According to mass action law, $n_0 p_0 = n_i^2$ in a semiconductor under thermal equilibrium.
2. It is valid at a constant temperature.
3. It is valid for degenerative semiconductors also.

Which of the above statements is/are true?
(a) 1 only (b) 2 only
(c) 1 and 2 only (d) 1, 2 and 3

202. **(c)**
Mass action law is not valid for degenerating type semiconductors. Because of doping upto degenerate level, the energy gap decreases. Hence intrinsic carrier concentration changes.

Q.203 Consider the circuit shown in the figure below



If diode D_1 and D_2 are made up of same material with the cut-in voltage V_γ = 0.7 V, then the value of current I is equal to
(a) 0.46 mA (b) 0.99 mA
(c) 0.59 mA (d) 1.06 mA

203. **(d)**
When D_2 is ON then the value of V_0 will be
$$V_0 = 3 - 0.7 \text{ V} = 2.3 \text{ V}$$

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Hence, D_1 will be OFF.

Thus, The current, $I = \frac{2.3-(-3)}{5}\times 10^{-3} = \frac{5.3}{5}\times 10^{-3} = 1.06$ mA

Q.204 Which of the following type of filter is suitable for small values of load resistance

(a) Capacitive filter (b) Inductive filter

(c) LC filter (d) None of these

204. (b)

In an inductive filter,

Ripple factor $\propto R_L$ (Load Resistance).

Thus if R_L is low then the ripple factor will also be less providing a good DC output.

Q.205 For an *n-p-n* transistor operating at constant collector current, for every 1°C rise in temperature.

(a) The base-emitter voltage increases by 2 mV

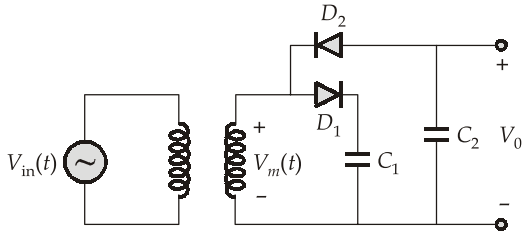
(b) The base-emitter voltage decreases by 2 mV

(c) The base-emitter voltage increases by 2.5 mV

(d) The base-emitter voltage decreases by 5 mV

205. (b)

Q.206 Consider the circuit shown in the figure below:



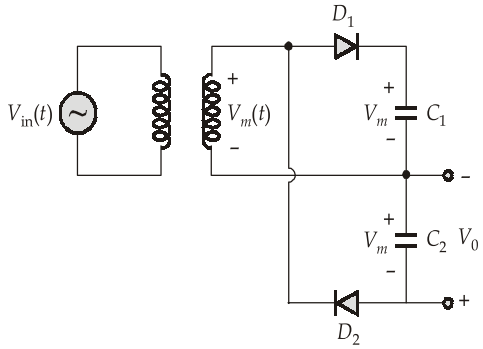
If the value of voltage on the secondary side of transformer is $V_m(t) = V_m \sin(\omega t)$, then the value of V_0 is equal to

(a) $0.5V_m$ (b) $2V_m$

(c) V_m (d) $-V_m$

206. (d)

The circuit can be redrawn as,



The circuit represents a voltage doubler circuit, if the voltage was taken by adding voltages of both the capacitors, but to calculate V_0 we have to find the voltage stored on a single capacitor. Thus, comparing from the above figure,

$$V_0 = -V_m$$

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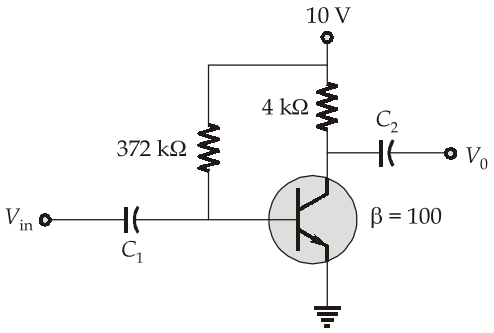
Q.207 Consider an amplifier circuit shown in the figure below:

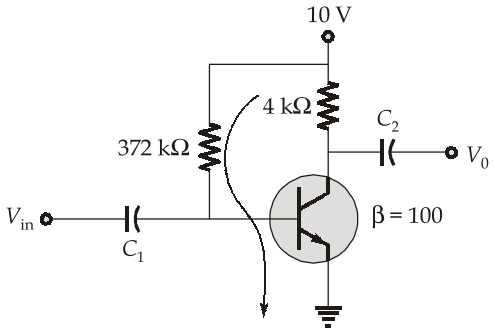


The voltage gain of the circuit is equal to
(Assume V_T = 25 mV and V_{BE} = 0.7 V)

(a) 415 (b) –200
(c) –400 (d) –210

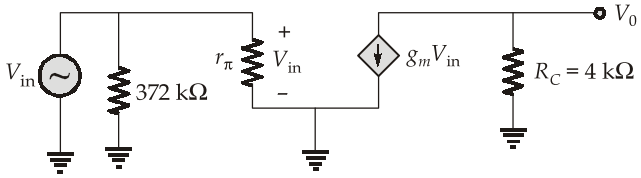
207. (c)

Applying KVL in base-emitter loop, we get,



$$I_B = \frac{10-0.7}{372\,\text{k}\Omega} = 25\,\mu\text{A}$$

To draw the small signal we need to calculate r_π



$$\therefore \quad r_\pi = \frac{V_T}{I_{B_{DC}}} = \frac{25\times10^{-3}}{25\times10^{-6}} = 10^3\ \Omega$$

now, $$g_m = \frac{\beta}{r_\pi} = \frac{100}{10^3} = 0.1\ \text{A/V}$$

now, $$A_v = \frac{V_0}{V_{in}} = -g_m R_C = -0.1\times4\times10^3 = -400$$

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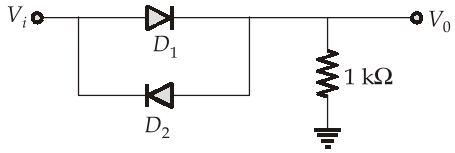
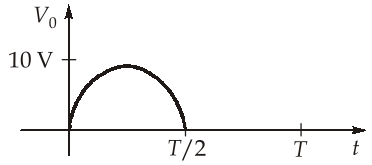
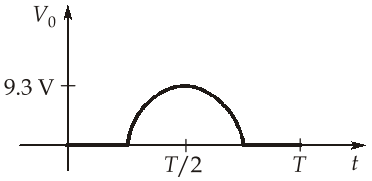
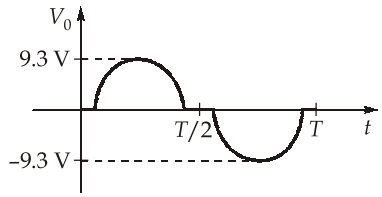
Q.208 Consider the circuit shown below:

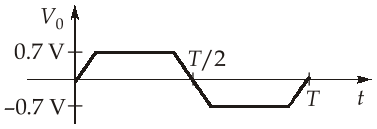


The diodes D_1 and D_2 are made up of silicon with cut-in voltage equal to 0.7 V. If input voltage $V_i = 10\sin(\omega t)$ V, then the signal wave at the output (V_0) will be equal to

(a)


(b)


(c)


(d)


208. (c)

For $V_i > 0$ V, Diode D_1 will switch ON after 0.7 V, and after that, $V_0 = V_i - 0.7$ V

For $V_i < 0$ V, Diode D_2 will switch ON for $V_i < -0.7$ V and $V_0 = V_i + 0.7$ V

Q.209 A particular *n-p-n* transistor is operating at $V_{BE} = 670$ mV, $I_C = 3$ mA and the $I_C - V_{CB}$ characteristic curve has a slope of 3×10^{-5} ℧ of constant I_B. Then the value of early voltage V_A for the transistor is equal to

(a) 50 V (b) 100 V

(c) 150 V (d) 200 V

209. (b)

The early voltage V_A can be calculated as

$$V_A = r_0 I_C$$

where r_0 = output resistance = $\dfrac{1}{\text{slope of } I_C - V_{CB} \text{ curve}}$

$$r_0 = \frac{1}{3\times10^{-5}}$$

thus, $$V_A = \frac{1}{3\times10^{-5}} \times 3\times10^{-3} = 100 \text{ V} \qquad (\because I_C = 3 \times 10^{-3} \text{ A})$$

Q.210 In a single time constant equivalent circuit of an amplifier, the pole is located at the left side of the $j\omega$ axis in the s-plane. If a negative feedback is applied to the circuit then

(a) The close loop pole will shift towards the right

(b) The close loop pole will not shift from its position

(c) The close loop pole will shift towards the left

(d) none of the above

210. (c)

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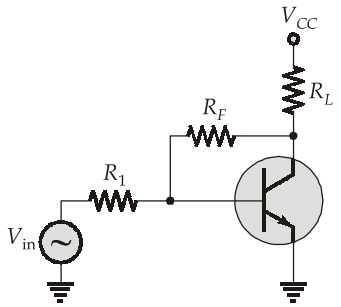
Q.211 Consider the circuit shown in the figure below:



If R_F represents the feedback resistor then, the feedback topology for the transistor amplifier is

(a) Voltage series
(b) Voltage shunt
(c) Current series
(d) Current shunt

211. (b)

Q.212 In a BJT amplifier, the capacitor that produces on A.C ground in a common emitter configuration is called as

(a) input coupling capacitor
(b) output coupling capacitor
(c) bypass capacitor
(d) none of the above

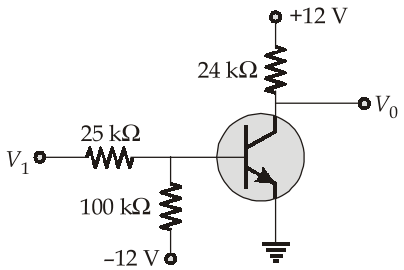
212. (c)

Q.213 The desirable characteristics of a transconductance amplifier are

(a) high input resistance and high output resistance
(b) high input resistance and low output resistance
(c) low input resistance and high output resistance
(d) low input resistance and low output resistance

213. (a)

Q.214 Consider the circuit shown below:



If the value of output voltage V_0 = 6 V and value of β = 100 and $V_{BE(ON)}$ = 0.7 V, then the value of input voltage V_1 is approximately equal to

(a) 0.7 V
(b) 13.12 V
(c) 10.16 V
(d) 3.94 V

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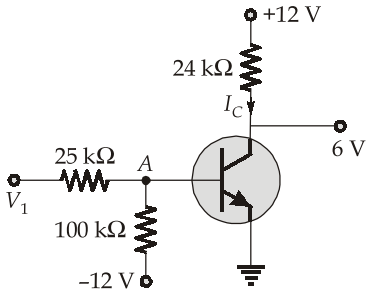
214. (d)

$$I_C = \frac{12-6}{24\,\text{k}\Omega} = \frac{6}{24\,\text{k}\Omega} = \frac{1}{4}\,\text{mA} = 0.25\,\text{mA},$$

Thus $I_B = 2.5\,\mu\text{A}$

Now, applying KCL at node A, we have



$$\frac{V_A - V_1}{25\,\text{k}\Omega} + \frac{V_A + 12}{100\,\text{k}\Omega} + 2.5\,\mu\text{A} = 0$$

$$4V_A - 4V_1 + V_A + 12 + 0.25 = 0$$

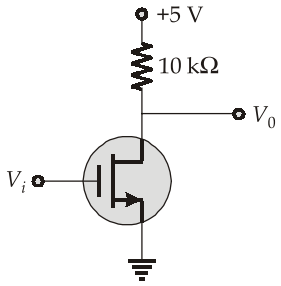
$$5V_A + 12 + 0.25 = 4V_1$$

$V_A = V_{BE(ON)} = 0.7$ V.

$$3.5 + 12 + 0.25 = 4V_1$$

$$V_1 = \frac{15.75}{4}\,\text{V} \approx 3.94\,\text{V}$$

Q.215 Consider the inverter circuit shown below:



The input voltage applied to the transistor V_i is equal to 4.2 V. The transistor has parameter $V_{TN} = 0.8$ V and $\mu_n C_{ox} = 20\,\mu\text{A/V}^2$. If the output voltage of the transistor V_0 is 0.1 V, then the value of (W/L) is approximately equal to

(a) 84 (b) 73

(c) 123 (d) 65

215. (b)

$$I_D = \frac{5-0.1}{10\,\text{k}\Omega} = 0.49\,\text{mA}$$

$\because$ $V_{DS} \le V_{GS} - V_{TN}$

Thus the transistor is operating in linear region.

$$\therefore \quad 0.49 \times 10^{-3} = \frac{20\times10^{-6}}{2} \times \left(\frac{W}{L}\right)\left[2(4.2-0.8)\,0.1 - (0.1)^2\right]$$

$$49 = \left(\frac{W}{L}\right)(0.67)$$

$$\therefore \quad \frac{W}{L} = \frac{49}{0.67} \approx 73$$

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Q.216 Which of the following conversion formulas of hybrid parameters hold true, for small-signal analysis of a BJT?

(a) $h_{ic} = 1 + h_{ie}$ (b) $h_{oc} = h_{ob}$

(c) $h_{ib} = \dfrac{h_{ie}}{1+h_{fe}}$ (d) $h_{fb} = h_{fe} + 1$

216. (c)

Q.217 In an RC coupled amplifier, the gain decreases due to

(a) coupling capacitance at low frequency and junction capacitance at high frequency.
(b) coupling capacitance at high frequency and bypass capacitance at low frequency.
(c) junction capacitance at low frequency and coupling capacitance at high frequency.
(d) none of the above is true.

217. (a)

Q.218 The output of an op-amp can increase maximum by 15 V in 12 μsec in response to an input test signal. Then the value of slew rate of the op-amp is equal to

(a) 1.25 V/ms (b) 2.35 V/ms
(c) 152.3 V/ms (d) 1250 V/ms

218. **(d)**

$$\text{Slew rate} = \left|\frac{\Delta V_{out}}{\Delta \text{time}}\right|_{max} = \frac{15\text{ V}}{12\,\mu\text{s}} = 1.25\text{ V}/\mu\text{s} = 1250\text{ V/ms}$$

Q.219 An amplifier has open-loop gain of 100 ± 10. Negative feedback is provided such that the closed-loop gain variation remains within ±1% from its nominal value. The feedback factor β is

(a) 0.09 (b) 0.90
(c) 0.01 (d) 0.11

219. **(a)**

$$A_f = \frac{A}{1+A\beta} \quad \ldots(i)$$

$$\frac{\partial A_f}{\partial A} = \frac{1}{(1+A\beta)^2} \quad \ldots(ii)$$

$$\frac{\partial A_f}{A_f} = \frac{\partial A}{A}\left(\frac{1}{1+A\beta}\right)$$

$$\frac{1}{100} = \frac{10}{100}\left(\frac{1}{1+100\beta}\right)$$

$$1 + 100\beta = 10$$

$$100\beta = 9$$

$$\beta = \frac{9}{100} = 0.09$$

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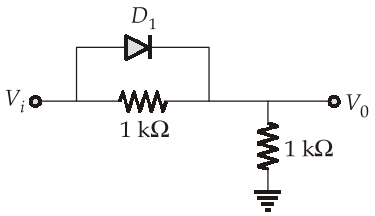
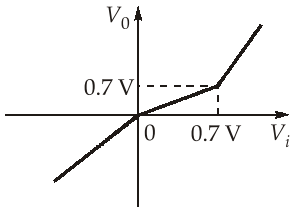
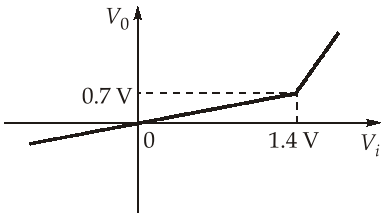
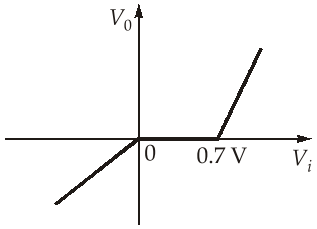
Q.220 Consider the diode circuit shown below:

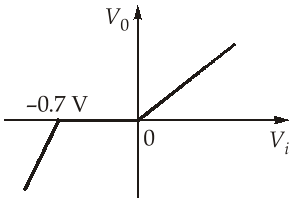


The transfer characteristic curve of the circuit can be represented as (Assume that the cut-in voltage of the diode is V_γ = 0.7 V)

(a)


(b)


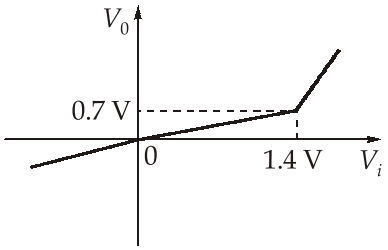
(c)


(d)


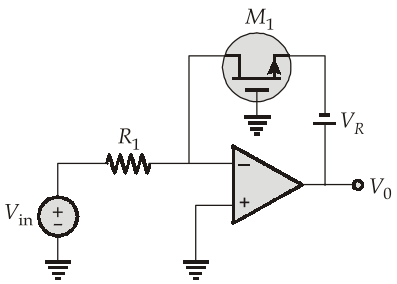
220. (b)

The graph can be broken down into two regions:

1. The diode D_1 is OFF, then $V_0 = \frac{1}{2}V_{in}$.
2. When diode D_1 is ON. (i.e., when $V_{in} > 1.4$ V), then $V_0 = V_{in} - 0.7$ V



Q.221 Consider an ideal op-amp based circuit shown below:



If the MOS is working in saturation region, then the circuit will work as a

(a) Logarithm amplifier
(b) Precision rectifier
(c) Square root amplifier
(d) Voltage follower

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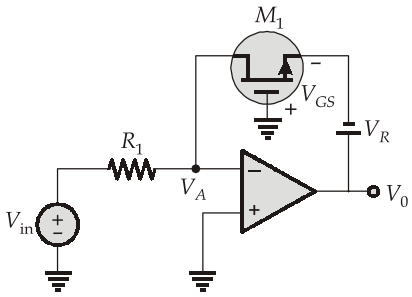
221. (c)



$$V_0 = -V_{GS} + V_R$$

For the MOS transistor, $I_D = k_n(V_{GS} - V_T)^2$

$$\sqrt{\frac{I_D}{k_n}} = V_{GS} - V_T$$

$$V_{GS} = \sqrt{\frac{I_D}{k_n}} + V_T$$

Now, from the given figure,

$$I_D = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \qquad (V_A = 0 \text{ due to Virtual ground})$$

$$\therefore \quad V_{GS} = \sqrt{\frac{V_{in}}{R_1 k_n}} + V_T$$

If V_R and R_1 are selected such that , $V_R = V_T$ and $R_1 k_n = 1$, then

$$V_0 = -\sqrt{V_{in}}$$

Q.222 A JFET amplifier is biased at $V_{GSQ} = -2$ V and, it has $I_{DSS} = 8$ mA and $V_p = -8$ V. Then the value of transconductance g_m offered by the JFET is equal to

(a) 2 mS (b) 1.5 mS
(c) 3.5 mS (d) 5 mS

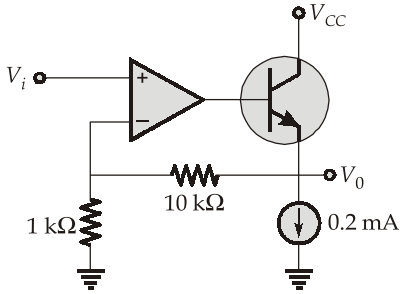
222. (b)

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

$$g_{mo} = \frac{2I_{DSS}}{|V_p|} = \frac{2\times(8\times10^{-3})}{8} = 2 \text{ mS}$$

$$\therefore \quad g_m = 2\left(1 - \frac{(-2)}{(-8)}\right) \text{mS} = 1.5 \text{ mS}$$

Q.223 Consider the circuit shown below:



Then the feedback circuit will behave as a

(a) Series-series feedback (b) Series-shunt feedback
(c) Shunt-series feedback (d) Shunt-shunt feedback

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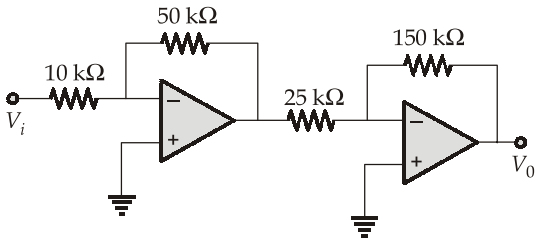
223. (b)

The output V_0 is sampled with the help of the two resistance of 10 kΩ and 1 kΩ and then added to the input.

Q.224 Consider the circuit shown below:



If the input voltage V_i is equal to 0.2 V and the op-amps are ideal, then the value of V_0 is equal to

(a) 3 V (b) 4 V

(c) 5 V (d) 6 V

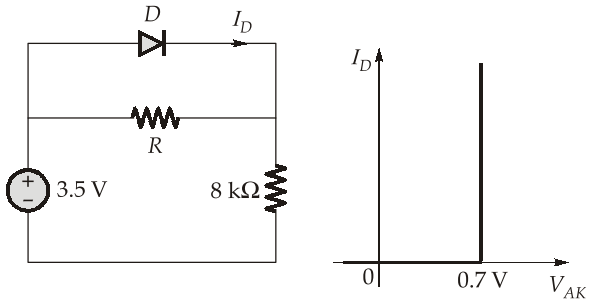
224. (d)

The two amplifiers have no cascading effect (∵ the op-amps are ideal).

Thus, $$A_V = A_1 \cdot A_2 = \left(-\frac{50}{10}\right)\left(-\frac{150}{25}\right) = -5 \times -6 = 30$$

$\therefore$ $$V_0 = 30 \times 0.2 = 6 \text{ V}$$

Q.225 Consider the circuit shown below along with the diode characteristics:



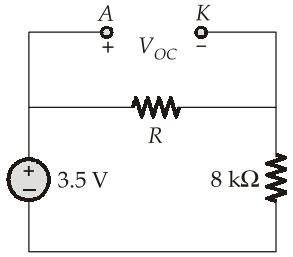
The diode in the above circuit will conduct (i.e. $I_D > 0$) for

(a) $R > 2$ kΩ (b) $R < 2$ kΩ

(c) $R > 6$ kΩ (d) $R < 6$ kΩ

225. (a)

Let us take the open circuit test,



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For diode to be in ON state,

$$V_{OC} > 0.7 \text{ V}$$

$$\frac{R}{R+8\text{k}\Omega}(3.5) > 0.7$$

$$\frac{R+8\text{k}\Omega}{R} < 5$$

$$\frac{8\text{k}\Omega}{R} < 4$$

$$R > 2 \text{ k}\Omega$$

Direction (Q.226 to Q.230): The following items consists of two statements, one labelled as **Statement (I)** and the other labelled as **Statement (II)**. You have to examine these two statements carefully and select your answers to these items using the codes given below:

Codes:

(a) Both Statement (I) and Statement (II) are true and Statement (II) is the correct explanation of Statement (I).

(b) Both Statement (I) and Statement (II) are true but Statement (II) is not a correct explanation of Statement (I).

(c) Statement (I) is true but Statement (II) is false.

(d) Statement (I) is false but Statement (II) is true.

Q.226 Statement (I): The junction capacitance is associated with a reverse biased *pn* junction due to the dipole in the transition region.

Statement (II): In a reverse biased *pn* junction, the uncompensated acceptor ions on the *p*-side provide a negative charge, and an equal positive charge results from the ionized donors on the *n*-side of the transition region.

226. (a)

Q.227 Statement (I): In a tunnel diode, isolation is not possible between input and output.

Statement (II): In a tunnel diode, peak current (I_p) is greater than valley current (I_v).

227. (b)

Q.228 Statement (I): In an intrinsic semiconductor, contribution to electrical conductivity by the electrons and holes is same.

Statement (II): In an intrinsic semiconductor, the number of electrons in the conduction band is equal to the number of holes in the valence band.

228. (d)

For an intrinsic semiconductor,

$$\sigma = ne\mu_n + pe\mu_p$$

$$n = p = n_i$$

But, $\mu_n \neq \mu_p$

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Q.229 **Statement (I):** In a RC-coupled amplifier, bypass capacitor serves the purpose of increasing the A.C. voltage gain of the amplifier.
Statement (II): Stabilization resistance R_E, necessarily introduces negative feedback for D.C. signal while the bypass capacitor eliminates the negative feedback for the A.C. signal.

229. (a)

Q.230 **Statement (I):** Class AB amplifier does not suffer from crossover distortion.
Statement (II): The output transistors of class AB amplifier are biased at a small quiescent current I_q and conducts for slightly more than half cycle.

230. (a)

■■■■

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