DETAILED SOLUTIONS

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ESE 2025 : Prelims Exam
CLASSROOM TEST SERIES

ELECTRICAL ENGINEERING

Test 2

Section A : Electrical Circuits

Section B : Digital Electronics + Microprocessors

ANSWER KEY

1. (a)	**16.** (a)	**31.** (a)	**46.** (c)	**61.** (c)
2. (a)	**17.** (c)	**32.** (b)	**47.** (d)	**62.** (c)
3. (d)	**18.** (a)	**33.** (b)	**48.** (d)	**63.** (b)
4. (a)	**19.** (c)	**34.** (b)	**49.** (d)	**64.** (d)
5. (d)	**20.** (c)	**35.** (c)	**50.** (a)	**65.** (b)
6. (b)	**21.** (a)	**36.** (d)	**51.** (d)	**66.** (c)
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8. (b)	**23.** (b)	**38.** (c)	**53.** (d)	**68.** (a)
9. (a)	**24.** (c)	**39.** (a)	**54.** (d)	**69.** (d)
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11. (b)	**26.** (b)	**41.** (b)	**56.** (d)	**71.** (c)
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DETAILED EXPLANATIONS
Section A : Electrical Circuits

1. (a)

By Applying current division rule

$$i_4 = 16 \times \frac{40}{40 + \frac{60R}{60+R}} \times \frac{R}{60+R} \qquad [\because 200 \,||\, 50 = 40\ \Omega]$$

$$4 = \frac{640(60+R)}{2400 + 40R + 60R} \times \frac{R}{(60+R)}$$

$$4 = \frac{640R}{2400 + 100R}$$

$$R = 40\ \Omega$$

2. (a)

Applying KVL,

$$\frac{V-24}{250} + \frac{V}{50} + \frac{V - 6I_b}{150} = 0$$

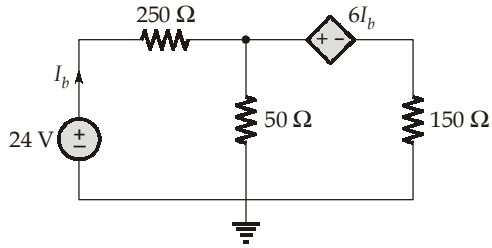
$$\frac{V-24}{250} + \frac{V}{50} + \frac{256V - 144}{37500} = 0 \qquad \left(\because I_b = \frac{24-V}{250}\right)$$

$$V = 3.24\ \text{V}$$

$$I_b = \frac{24 - 3.24}{250}$$

$$P_{24V} = 24 \times \frac{(24 - 3.24)}{250}$$

$$= 1.99\ \text{W}$$



3. (d)

An ideal voltage source produces a specific potential difference across its terminals regardless of what is connected to it. An ideal current source produces a specific current through its terminals regardless of what is connected to it.

4. (a)

Kirchhoff's voltage law is based on the principle of conservation of energy.

5. (d)

- A capacitor is an open circuit to dc.
- The voltage on a capacitor cannot change abruptly
- The equivalent capacitance of N parallel-connected capacitors is the sum of the individual capacitances.
- The reciprocal of the equivalent capacitance of series-connected capacitors is the sum of the reciprocals of the individual capacitances.

6. (b)

By Millman's theorem, equivalent voltage,

$$V = \frac{\sum_{i=1}^{5} EiYi}{\sum_{i=1}^{5} Yi} = \frac{1\times1 - 2\times\frac{1}{2} + 3\times\frac{1}{3} - 4\times\frac{1}{4} + 5\times\frac{1}{5}}{1+\frac{1}{2}+\frac{1}{3}+\frac{1}{4}+\frac{1}{5}} = \frac{60}{137}\text{V}$$

$$\frac{1}{Z} = \frac{1}{Z_1}+\frac{1}{Z_2}+\frac{1}{Z_3}+\frac{1}{Z_4}+\frac{1}{Z_5}$$

$$\frac{1}{Z} = \frac{1}{1}+\frac{1}{2}+\frac{1}{3}+\frac{1}{4}+\frac{1}{5}$$

$$\Rightarrow \quad Z = \frac{60}{137}\Omega$$

Therefore, the current through the 6 Ω resistance,

$$I = \frac{V}{Z+6} = \frac{\frac{60}{137}}{\frac{60}{137}+6} = \frac{60}{882}\text{A}$$

Hence the voltage between the points F and G is

$$V_{FG} = 6\times I = 6\times\frac{60}{882} = \frac{60}{147}\text{V}$$

7. (c)

The characteristic equation defining the behavior of a source-free series RLC circuit is given by:

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$$

where, $\quad 2\xi\omega_n = \frac{R}{L}$

and $\quad \omega_n = \frac{1}{\sqrt{LC}}$

$$\Rightarrow \quad \xi = \frac{R}{2}\sqrt{\frac{C}{L}}$$

For underdamped case, $\xi < 1$

$$\Rightarrow \quad \frac{R}{2}\sqrt{\frac{C}{L}} < 1$$

$$\Rightarrow \quad \frac{R^2}{4L^2} < \frac{1}{LC}$$

8. (b)

At resonant frequency, the inductive and capacitive reactances are equal so that current and voltage are in phase. For any frequency lower than the resonant frequency, the inductive reactance is less than the capacitive reactance and hence the circuit behaves as a capacitive circuit.

Quality factor is inversely proportional to R. Hence for a series RLC circuit, a high value of quality factor implies low losses and a low value of Q implies high losses.

9. (a)

By KVL for three meshes we get,

$$V_1 = 10I_1 + 3I_2 + 2(I_1 + I_2) = 12I_1 + 5I_2 \quad \ldots(i)$$

$$V_2 = 2(I_2 - 2V_3) + 2(I_1 + I_2)$$

$$= 2I_1 + 4I_2 - 4V_3 \quad \ldots(ii)$$

Also, $V_3 = 2(I_1 + I_2) = 2I_1 + 2I_2$ ...(iii)

From (ii) and (iii)

$$V_2 = 2I_1 + 4I_2 - 4(2I_1 + 2I_2)$$

$$= -6I_1 - 4I_2 \quad \ldots(iv)$$

From (i) and (iv), we get

$$Z = \begin{bmatrix} 12 & 5 \\ -6 & -4 \end{bmatrix}$$

10. (c)

Both statements are correct.

11. (b)

Here, the turns ratio, $n = 10$, Load impedance = R

$\therefore$ Referred impedance, $Z = \dfrac{Z_L}{n^2} = \dfrac{R}{10^2}$

$\therefore$ Primary current, $I_1 = \dfrac{50}{100 + \dfrac{R}{100}}$

$\therefore$ Secondary current, $I_2 = \dfrac{I_1}{n} = \dfrac{5}{100 + \dfrac{R}{100}}$

$\therefore$ Average power dissipated in the resistor is

$$P = |I_2|^2 \times R$$

$$6.25 = \frac{25}{\left(100 + \dfrac{R}{100}\right)^2} \times R$$

$$\left(100 + \frac{R}{100}\right)^2 = 4R$$

$$R = 10 \text{ k}\Omega$$

12. (b)

If the self self-inductances are L_1 and L_2 and mutual inductance is M then,

$$L_1 + L_2 + 2M = 0.6 \quad \ldots(i)$$

And $$L_1 + L_2 - 2M = 0.1 \quad \ldots(ii)$$

Also, it is given that $L_1 = 0.2$ H. Putting this value in (i) and (ii)

$$\therefore \quad L_2 + 2M = 0.4 \quad \ldots(iii)$$

$$L_2 - 2M = -0.1 \quad \ldots(iv)$$

Solving (iii) and (iv), we get

$$L_2 = 0.15 \text{ H}, M = 0.125 \text{ H}$$

$\therefore$ Coefficient of coupling is

$$K = \frac{M}{\sqrt{L_1 L_2}} = \frac{0.125}{\sqrt{0.2 \times 0.15}} = 0.721$$

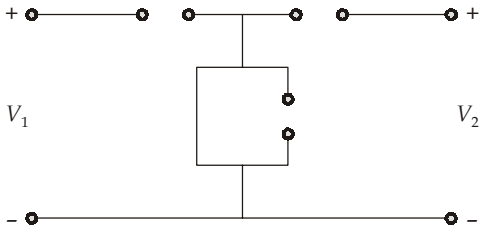
13. (c)

At $\omega = 0$,

i.e., $f = 0$

$$X_L = 0$$

$$X_C = \infty$$



There is no connection between input and output,

So, $V_2 = 0$

At $\omega = \infty$,

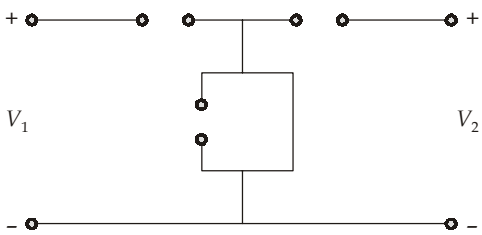
i.e. $f = \infty$,

$$X_L = \infty$$

$$X_C = 0$$

Then also, there is no connection between input and output,

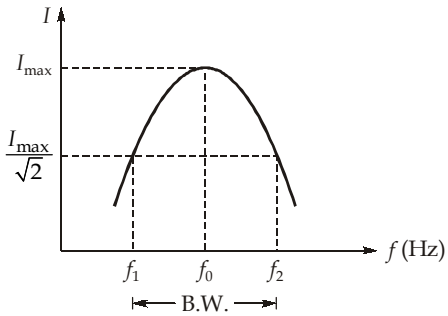
So, $V_2 = 0$



Band pass filter.

14. (a)

The bandwidth is the range of frequencies in which the power level in the signal is atleast half of the maximum power.



At the corner frequencies f_1 and f_2 , power absorbed by the resistance, R is

$$P = \left(\frac{I_{max}}{\sqrt{2}}\right)^2 R = \frac{I_{max}^2 R}{2} = 0.5P_{max}$$

where, $P_{max} = I_{max}^2 R$

15. (a)

Properties of complete incidence matrix.

- The sum of the entries in any column is zero.
- The determinant of the incidence matrix of a closed loop is zero.
- The rank of the incidence matrix of a connected graph is $(n - 1)$.

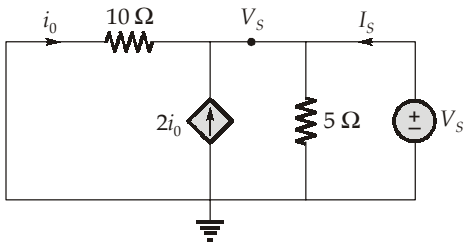
16. (a)

In a graph, the number of links is calculated as $b - n + 1$

where 'b' is the total number of branches in the graph and 'n' is the number of nodes.

17. (c)

To find R_{Th} , deactivate 180 V source, (independent source) and cannot a test source connect a test source voltage delivering I_S current.



KCL :

$$i_0 + 2i_0 + I_S = \frac{V_S}{5}$$

$$3i_0 + I_S = \frac{V_S}{5}$$

$$3\left[\frac{0-V_S}{10}\right]+I_S = \frac{V_S}{5}$$

$$\therefore \quad R_{Th} = \frac{V_S}{I_S} = 2\ \Omega$$

18. (a)

Tellegen's theorem is applicable under all conditions, including sinusoidal steady-state conditions. If the network is in sinusoidally steady state (ac circuits) then Tellegen's theorem is given as

$$\sum_{K=1}^{b} V_k I_K^* = 0$$

19. (c)

Ohm's law cannot be applied to open circuit and short circuit, it must have some finite resistance.

20. (c)

Superposition theorem cannot be applied when

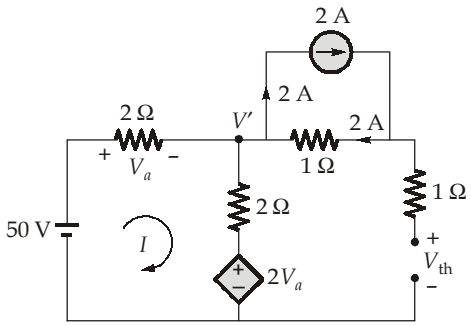
- Two ideal voltage sources are connected in parallel because KVL will not be satisfied.
- Two ideal current sources are connected in series because KCL will not be satisfied.

21. (a)

- The resultant impedance parameter matrix for the series connection is the addition of the two individual impedance matrices.
- The resultant hybrid parameter matrix for the series-parallel connection is the addition of the two individual hybrid parameter matrices.
- The resultant inverse hybrid parameter matrix for the parallel-series connection is the addition of the two individual inverse hybrid parameter matrices.

22. (c)

Disconnecting the load resistance, we calculate the Thevenin voltage across the open circuit terminals.



$$2I = V_a$$

by using KVL, $\quad 50 - 2V_a = 4I$

$$50 = 4I + 4I$$

$$8I = 50$$

$$I = \frac{50}{8} = \frac{25}{4}\text{A}$$

$$V' = 2I + 2V_a = 2I + 4I = 6I$$

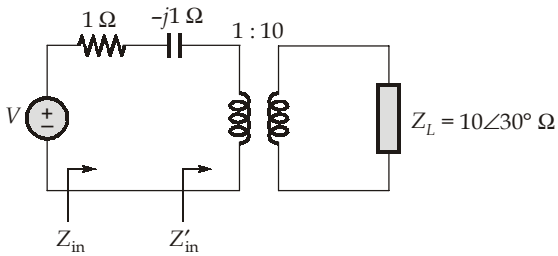
$$V' = \frac{25}{4} \times 6 = 37.5 \text{ volt}$$

$$V_{th} = 2 + V' = 2 + 37.5$$

$$V_{th} = 39.5 \text{ V}$$

23. (b)

Given, Circuit



The impedance seen by the source,

$$Z_{in} = 1 - j1 + Z'_{in}$$

where,
$$Z'_{in} = \left(\frac{N_1}{N_2}\right)^2 Z_L = \left(\frac{1}{10}\right)^2 10\angle 30°$$

$$Z'_{in} = 0.087 + j0.05$$

$$Z_{in} = 1 - j1 + 0.087 + j0.05$$

$\therefore$
$$Z_{in} = 1.087 - j0.95\ \Omega$$

24. (c)

For transient free response,

$$\omega t_0 = \tan^{-1}\left(\frac{\omega L}{R}\right)$$

$$R = 8\ \Omega \,||\, 8\ \Omega$$

$$R = 4\ \Omega$$

$$2t_0 = \tan^{-1}\left(\frac{2 \times 2}{4}\right)$$

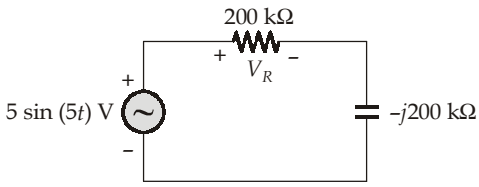
$$2t_0 = \tan^{-1}(1)$$

$$2t_0 = \frac{\pi}{4}$$

$$t_0 = \frac{\pi}{8} = \frac{3.14}{8} = 0.39 \text{ sec}$$

25. (b)

$$X_C = \frac{1}{\omega C} = \frac{1}{5\times10^{-6}} = 200\ \text{k}\Omega$$



$$\therefore \quad V_R = \frac{5\angle0°}{(200-j200)}\times200$$

$$= \frac{5\angle0°}{(1-j)} = \frac{5\angle0°}{\sqrt{2}\angle-45°} = 2.5\sqrt{2}\ \angle45°$$

$$V_R = 2.5\sqrt{2}\sin(5t+0.25\pi)\ \text{volt}$$

26. (b)

We know that,

Self inductance of a coil is, $L = \dfrac{\mu_0 N^2 A}{l}$

where, N is number of turns

$$\therefore \quad L \propto N^2$$

$$\frac{L_1}{L_2} = \left(\frac{N_1}{N_2}\right)^2$$

$$\frac{1}{0.25} = \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore \quad \frac{N_1}{N_2} = 2$$

27. (d)

For series RLC circuit, $\xi_1 = \dfrac{R}{2}\sqrt{\dfrac{C}{L}} = \dfrac{1}{2G}\sqrt{\dfrac{C}{L}}$

For parallel RLC circuit, $\xi_2 = \dfrac{1}{2R}\sqrt{\dfrac{L}{C}} = \dfrac{G}{2}\sqrt{\dfrac{L}{C}}$

when $G \uparrow$ then

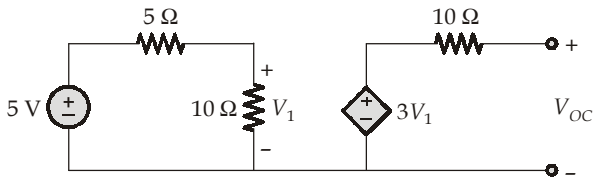
$\xi_1 \rightarrow$ Decreases

$\xi_2 \rightarrow$ Increases

28. (b)

From the given circuit, we have

$$V_1 = \frac{5\times10}{10+5} = \frac{50}{15} = \frac{10}{3}\text{ V}$$



$$\therefore \quad V_{OC} = 3V_1 = 3\times\frac{10}{3} = 10\text{ V}$$

$$I_{SC} = \frac{10}{10} = 1\text{ A}$$

$$\therefore \quad R_{Th} = \frac{V_{OC}}{I_{SC}} = 10\ \Omega$$

so,
$$P_{max} = \frac{V_{Th}^2}{4R_{Th}} = \frac{V_{OC}^2}{4R_{Th}} = \frac{10\times10}{4\times10} = 2.5\text{ W}$$

29. (a)

From the given characteristics, it is clear that,

when $V = 0$ V (short circuit)

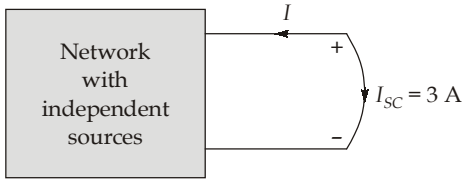
$I = -3$ A

and when $V = 15$ V

$I = 0$ A (open circuit)

$\therefore$ Network becomes,

$$V_{OC} = 15\text{ V}$$
$$I_{SC} = -I = 3\text{ A}$$



$$\therefore \quad R_{Th} = \frac{15}{3} = 5\ \Omega$$

and maximum power transferred is

$$P_{max} = \frac{V_{OC}^2}{4R_{Th}} = \frac{(15)^2}{4\times5} = \frac{15\times15}{20}$$

$$= \frac{45}{4} = 11.25\text{ W}$$

30. (a)

Here $Z_L = j\omega L = j \times 1000 \times 10^{-3} = j$

and $Z_C = \dfrac{1}{j\omega C} = \dfrac{-j}{1000 \times 10^{-3}} = -j$

$\therefore$ $Z_{eq} = 1 + (Z_L \,||\, Z_C)$

$= 1 + \dfrac{(j)(-j)}{-j + j} = 1 + \dfrac{1}{0} = \infty$

$\therefore$ $I = 0$

31. (a)

Here $v_0(t)$ is negative means current direction is opposite in the coils

$\therefore$ $v_0(t) = \dfrac{M\, di_1(t)}{dt}$

$M = \dfrac{|v_0(t)|}{\left|\dfrac{di_1(t)}{dt}\right|} = \dfrac{40}{16} = 2.5\ \text{H}$

32. (b)

The time constant for RC circuit is

$\tau = R_{eq}\, C_{eq}$

here, $R_{eq} = 2\ \Omega$

and $C_{eq} = \dfrac{(4\,\text{F} + 4\,\text{F})(8\,\text{F})}{(4\,\text{F} + 4\,\text{F}) + 8\text{F}} = \dfrac{8\,\text{F} \times 8\,\text{F}}{16\,\text{F}} = 4\,\text{F}$

$\therefore$ $\tau = 2 \times 4 = 8$ sec

33. (b)

From h-parameter model,

$V_1 = h_{11} I_1 + h_{12} V_2$ ...(i)

$I_2 = h_{21} I_1 + h_{22} V_2$ ...(ii)

From transmission parameter model,

$V_1 = A V_2 - B I_2$ ...(iii)

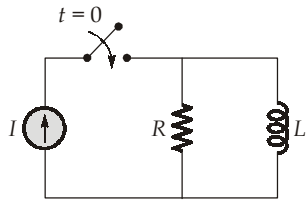
$I_1 = C V_2 - D I_2$ ...(iv)

where, $B = \left.\dfrac{-V_1}{I_2}\right|_{V_2 = 0}$ [From equation (iii)]

$\therefore$ From equation (i) and (ii), keeping $V_2 = 0$, we get,

$B = \dfrac{-h_{11}}{h_{21}}$

34. (b)

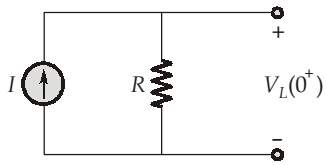


$t = 0^-$, the current through inductor is 0 A, i.e.,

$$i_L(0^-) = 0 \text{ A}$$

$t = 0^+$, Inductor acts as a O.C.

$$i_L(0^+) = 0 \text{ A},$$
$$V_L(0^+) = IR$$



$t \to \infty$, inductor acts as a short circuit and current 'I' flows through it and voltage across it is '0 V'

$$i_L(\infty) = I$$
$$v_L(\infty) = 0 \text{ V}$$

Energy stored in a inductor between time interval is $\frac{1}{2}LI^2$

$$\text{Expression for } v_L(t) = v_L(\infty) + (v_L(0^+) - v_L(\infty))e^{-t/\tau}$$
$$v_L(t) = IR\,e^{-(R/L)t},\ t \geq 0$$

The voltage across the supply is $v_L(t)$

The energy supplied by the source is

$$W_s = \int_0^\infty v_L \cdot I\,dt = \int_0^\infty IR\,e^{(-R/L)t} \cdot I\,dt = I^2L$$

The ratio of energy stored in a inductor to the energy supplied by the source is 0.5.

35. (c)

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad \ldots(\text{i})$$
$$I_2 = h_{21}I_1 + h_{22}V_2 \quad \ldots(\text{ii})$$

Write KVL equation in first loop,

$$V_1 = 20I_1 + (0)V_2$$

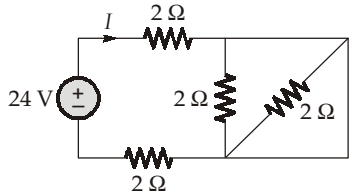
Write KCL equation at node,

$$I_2 = I_1(180) = 180I_1 + (0)V_2$$

Compare with equation (i) and (ii),

$$h = \begin{bmatrix} 20 & 0 \\ 180 & 0 \end{bmatrix}$$

36. (d)



$$R_{eq} = 2 + 2 = 4\ \Omega$$

$$I = \frac{24}{4} = 6\ \text{A}$$

37. (a)

A two-port network is resistive means it is a reciprocal network

$$AD - BC = 1$$

Condition for symmetrical,

$$A = D$$

From figure,

$$I_1 = 10\ \text{A}, \qquad V_1 = 19\ \text{V},$$
$$V_2 = 8\ \text{V}, \qquad I_2 = -1\ \text{A}$$
$$V_1 = AV_2 - BI_2 \quad \text{...(i)}$$
$$I_1 = CV_2 - DI_2 \quad \text{...(ii)}$$
$$19 = A(8) - B(-1) \quad \text{...(iii)}$$
$$10 = C(8) - D(-1) \quad \text{...(iv)}$$
$$10 = 8C + D \qquad (A = D)$$
$$10 = 8C + A$$
$$C = \frac{10 - A}{8} \quad \text{...(v)}$$

From equation (iii),

$$B = -8\ \text{A} + 19 \quad \text{...(vi)}$$

The circuit is resistive, so it is a reciprocal network,

$$AD - BC = 1 \quad \text{...(vii)}$$
$$A \cdot A - BC = 1$$
$$A^2 - BC = 1$$

Substitute equation (v) and equation (vi) in equation (vii),

$$A = 2, \qquad B = 3,$$
$$C = 1, \qquad D = A = 2$$
$$= \begin{bmatrix} 2 & 3 \\ 1 & 2 \end{bmatrix}$$

38. (c)

$$[G] = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}$$

$$I_1 = g_{11}V_1 + g_{12}I_2 \quad ...(i)$$

$$V_2 = g_{21}V_1 + g_{22}I_2 \quad ...(ii)$$

The y-parameter equations of the above network are

$$I_1 = \frac{2}{R}V_1 + \frac{1}{R}V_2 \quad ...(iii)$$

$$I_2 = \frac{1}{R}V_1 + \frac{2}{R}V_2 \quad ...(iv)$$

$$g_{12} = \left.\frac{I_1}{I_2}\right|_{V_1=0} = \frac{\frac{1}{R}V_2}{\frac{2}{R}V_2} = 0.5$$

$$g_{21} = \left.\frac{V_2}{V_1}\right|_{I_2=0} = \frac{\frac{-1}{R}}{\frac{2}{R}} \quad \text{[Using equation (iv)]}$$

$$= -0.5 = -g_{12}$$

40. (d)

Power factor in any circuit is given by cos ϕ where ϕ is the angle between voltage and current in the circuit.

∵ The voltage across and current through the capacitor are in phase quadrature.

∴ $\phi = 90°$

and $\cos 90° = 0$ (Power factor)

Section B : Digital Electronics + Microprocessors

41. (b)

We have, $X + Y = 8$ i.e., $X = 8 - Y$ ...(i)

$$(123(8 - Y))_8 = (Y03Y)_6$$

Now, on expanding the above given algebraic equation, we get

$$(8^3 \times 1) + (8^2 \times 2) + (3 \times 8) + 8 - Y = 6^3Y + (3 \times 6) + Y$$

$$512 + 128 + 24 + 8 - Y = 216Y + 18 - Y$$

On solving we get $Y = 3$

From eqn. (i) we get, $X = 8 - Y = 8 - 3 = 5$

42. (b)

The overflow occurrence is checked by the Boolean function

$$f(x, y, z) = \bar{x}\,\bar{y}\,z + x\,y\,\bar{z}$$

where x and y are the sign bit of additive operands and z is the sign bit of output that we get after the addition.

Now,

For $x = 1; y = 0; z = z$

$$f(x, y, z) = 0 \cdot 1 \cdot z + 1 \cdot 0 \cdot \bar{z} = 0$$

Therefore, no overflow will occur.

43. (b)

We know that,

From 'n' variable, 2^{2^n} number of distinct Boolean expressions can be formed.

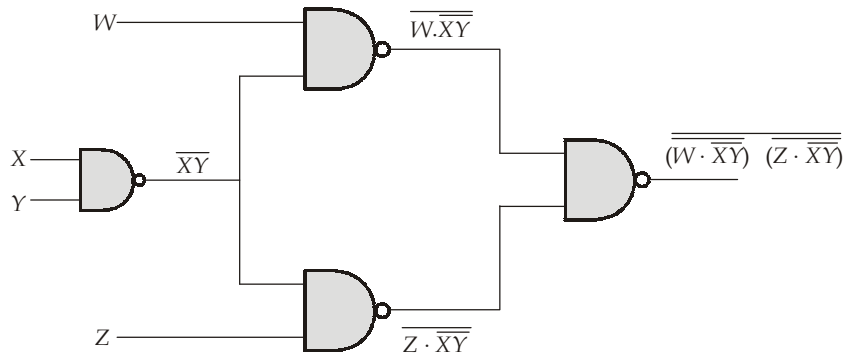
Thus, $2^{2^n} = 16$

$$2^{2^n} = 2^4$$
$$2^n = 4 = 2^2$$
$$n = 2$$

44. (a)

$$F(W, X, Y, Z) = W\bar{X} + \bar{Y}Z + W\bar{Y} + \bar{X}Z$$
$$= W(\bar{X} + \bar{Y}) + Z(\bar{X} + \bar{Y}) = (\bar{X} + \bar{Y})(W + Z)$$
$$= (\overline{XY})(Z + W) = \overline{XY}Z + \overline{XY}W$$

or $$F(W, X, Y, Z) = \overline{(\overline{\overline{XY}Z})(\overline{\overline{XY}W})} = \overline{XY}Z + \overline{XY}W$$



Thus, minimum number of NAND gates required to implement

$$F(W, X, Y, Z) = W\bar{X} + \bar{Y}Z + W\bar{Y} + \bar{X}Z \text{ is 4.}$$

45. (c)

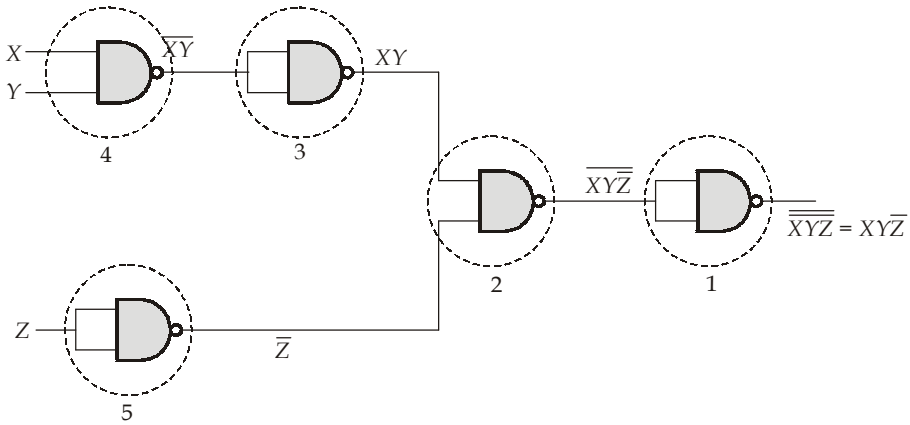
As, we know that

$$f_{clk} = \frac{1}{2Nt_{pdff}}$$

$$N = \frac{1}{2 \times f_{clk} \times t_{pdff}} = \frac{1}{2 \times 5 \times 10^{-9} \times 10 \times 10^{6}} = 10$$

46. (c)

$$F = XY\bar{Z}$$



Thus, minimum number of NAND gates required is 5.

47. (d)

We have,

Logic circuit	Number of NAND Gates required	Number of NOR Gates required
NOT	1	1
AND	2	3
OR	3	2
EX-OR	4	5
EX-NOR	5	4
NOR	4	1
NAND	1	4

48. (d)

- DTL suffers from large propagation delay owing to the need for the transistor base charge to leak out if the transistor were to switch from conducting to non-conducting state.
- ECL achieves its high-speed operation by preventing the transistors from entering the saturation region.

- An AND gate's output is high only when all of its inputs are high. If any input is low, the output will be low.

All the statements are correct. Therefore, option (d) is correct.

49. (d)

$$\text{Output voltage} = \frac{1}{2^N} \times (\text{decimal equivalent of digital (Binary) input}) \times V_{FS}$$

$$10 = \frac{1}{2^4} \times (\text{decimal equivalent of digital input}) \times 32$$

$$\frac{10\times16}{32} = (\text{decimal equivalent of digital input})$$

$$(5)_{10} = \text{decimal equivalent of digital input}$$

$\therefore$ Digital input = $(5)_{10} = (0101)_2$. Thus, answer is (d)

50. (a)

Truth table of SR flip-flop:

$S\ R$	Q_{n+1}
0 0	Q_n
0 1	0
1 0	1
1 1	Invalid state (Q becomes equal to $\bar{Q}$)

Thus, for input 00, SR flip-flop will uphold the previous output.

51. (d)

Output of 4 × 1 MUX,

$$F(A, B, C) = \bar{B}\bar{C}(A) + \bar{B}C(\bar{A}) + B\bar{C}(\bar{A}) + BC(A)$$

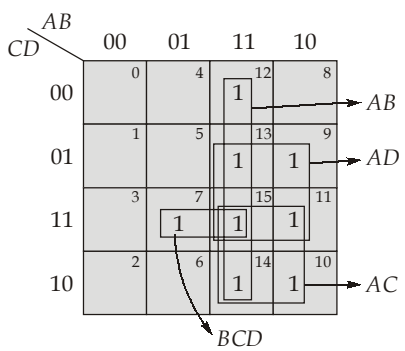
$$= A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC$$

$$F = \bar{B}(A \oplus C) + B(A \odot C)$$

$$F = \bar{B}(A \oplus C) + B(\overline{A \oplus C})$$

52. (b)

K-map for given expression can be drawn as:



K-map consists of three quads and one pair as shown above,

The simplified expression for *K*-map,

$$Y = AB + AD + AC + BCD$$

53. (d)

- TTL is the most popular bipolar logic family.
- ECL achieves high speed operation by employing a relatively small voltage swing and preventing the transistors from entering the saturation region.
- MOS and I^2L logic families have high packing density as they do not use resistors which reduces the overall circuit area and allows for higher packing density.

Hence, all the statements are correct.

54. (d)

Given, t_{pd} = 20 picoseconds

For the ripple counter to work properly,

$$T_{clk} \geq nt_{pd}$$

$$f_{clk} \leq \frac{1}{nt_{pd}}$$

Consider that the, MOD 64 counter requires 'n' JK flip-flops, then we have

$$N \leq 2^n$$

$$64 \leq 2^n$$

$$\therefore \quad n = 6$$

$$f_{clk} \leq \frac{1}{6 \times 20 \times 10^{-12}}$$

$$f_{clk} \leq \frac{10^{12}}{120}$$

$$f_{clk}(\max) = 8.33 \text{ GHz}$$

55. (b)

Total number of bits in the memory

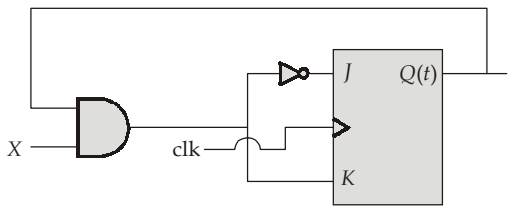
$= 2^n \times m$, where 'n' are the address bits and 'm' are the data bits

$= 2^{12} \times 8$

$= 4096 \times 8$ bits $= 4096$ bytes

56. (d)

The given circuit can be redrawn as



$$J = \overline{XQ(t)};\ K = XQ(t)$$

$$\therefore \quad Q(t+1) = J\overline{Q(t)} + \overline{K}Q(t)$$

$$= \overline{XQ(t)} \cdot \overline{Q(t)} + \overline{XQ(t)} \cdot Q(t)$$

$$= \overline{XQ(t)}\left[\overline{Q(t)} + Q(t)\right]$$

$$= \overline{XQ(t)} \cdot [1]$$

$$Q(t+1) = \overline{X} + \overline{Q(t)}$$

57. (d)

Given, $Y = \overline{A} + BC$

A \ BC	00	01	11	10
0	1	1	1	1
1			1	

$\therefore \quad Y = \Sigma m(0, 1, 2, 3, 7)$

(or) $\quad Y = \pi M(4, 5, 6)$

58. (d)

- Successive Approximation ADC: $T_{conv} = nT_{clk}$
- Parallel Comparator ADC: $T_{conv} = T_{clk}$
- Counter ramp ADC: Tconv = $2^n\ T_{clk}$
- Dual slope ADC: $T_{conv} = 2^{N+1}\ T_{clk}$

Thus, the dual slope ADC has the highest conversion time resulting in the minimum speed of conversion.

59. (a)

Given, output voltage, $V_0 = 3$ V

We know that,

output = resolution × (Decimal equivalent)

For an input of $(0110)_2 = (6)_{10}$,

$3 = \text{Resolution} \times 6$

$\therefore \quad \text{Resolution} = \dfrac{3}{6} = 0.5\ \text{V}$

For an input code of $(1001)_2$,

output voltage, V_0' = Resolution × (Decimal equivalent of 1001)

$\therefore \quad V_0' = 0.5 \times 9 = 4.5\ \text{V}$

60. (b)

- SRAM is faster and more expensive than DRAM.
- Each memory cell in DRAM consists of a single transistor and a capacitor whereas each memory cell in SRAM typically consists of six transistors. Thus, DRAM has higher bit density than SRAM.

61. (c)

$$P(x) = x^5 + 8x^3 + x$$
$$= x[x^2 (x^2 + 8) + 1]$$

Let A be the temporary variable to store the result. The arithmetic operations required to evaluate the polynomial is given by

1. $A = x * x$
2. $A = A + 8$
3. $A = x * A$
4. $A = x * A$
5. $A = A + 1$
6. $A = x * A$

Therefore, the minimum number of operations required = 6.

62. (c)

Both the statements are correct.

63. (b)

Memory capacity = 72 GB

$2^n \rightarrow$ Memory size (where n : no. of address lines)

$2^n \geq 72$ GB

$2^n \geq 72 \times (2^{30})$B

$\geq 2^7 \times 2^{30}$B

$2^n \geq 2^{37}$B

$\therefore \quad n \geq 37$

Minimum, $n = 37$

64. (d)

- Memory has separate address and data lines.
- Processor does not have separate address and data lines. The lower 8 lines are multiplexed which can be used either as address or data bus.

65. (b)

Program counter is a 16-bit register which contains the address of next instruction to be executed or it takes care of program flow/control.

66. (c)

In cycle stealing mode, the interference is less.

67. (c)

RAL → affects only carry flag
MOV B → affects no flag
ACI → affects all flag
INR M → All flags except carry flag are affected.

68. (a)

H and L register are known as primary data registers.

69. (d)

CALL is a 3-byte instruction.

70. (a)

To find address of RST 4.5, multiply 4.5 by 8

i.e., $4.5 \times 8 = (36)_{10}$

$= (24)_H$

71. (c)

RLC → rotate the content of 'A' 1-bit left without carry.
RRC → rotate the content of 'A' 1-bit right without carry.
RAL → rotate the content of 'A' 1-bit left with carry.
RAR → rotate the content of 'A' 1-bit right with carry.

72. (c)

8085 microprocessor uses multiplexed 8 lines for data bus.

73. (c)

XCHG exchanges the content of DE and HL pair registers,

So, after XCHG instruction is executed,

DE : $(40\ 30)_H$
HL : $(20\ 10)_H$

74. (d)

DMA (Direct Memory Access) is a process where data is transferred between two peripherals without the involvement of microprocessor.

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