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ESE 2025 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

Section A : Network Theory

Section B : Digital Circuits

1.	**(c)**	**16.**	**(c)**	**31.**	**(d)**	**46.**	**(d)**	**61.**	**(d)**
2.	**(b)**	**17.**	**(d)**	**32.**	**(a)**	**47.**	**(b)**	**62.**	**(c)**
3.	**(d)**	**18.**	**(d)**	**33.**	**(c)**	**48.**	**(b)**	**63.**	**(a)**
4.	**(b)**	**19.**	**(b)**	**34.**	**(d)**	**49.**	**(a)**	**64.**	**(a)**
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11.	**(a)**	**26.**	**(b)**	**41.**	**(a)**	**56.**	**(b)**	**71.**	**(a)**
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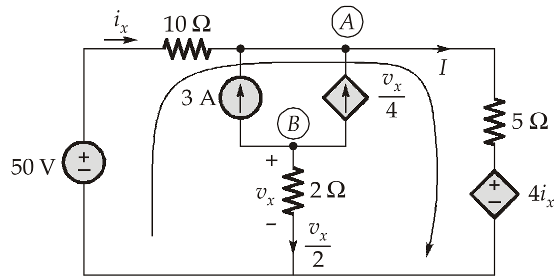
14.	**(c)**	**29.**	**(d)**	**44.**	**(d)**	**59.**	**(b)**	**74.**	**(b)**
15.	**(b)**	**30.**	**(b)**	**45.**	**(b)**	**60.**	**(c)**	**75.**	**(a)**

Section A : Network Theory

1. (c)



Apply KCL at node B,

$$\frac{v_x}{2}+\frac{v_x}{4}+3 = 0$$

$$v_x\left(\frac{1}{2}+\frac{1}{4}\right) = -3$$

⇒ $$v_x = -4 \text{ V}$$

Apply KCL at node A,

$$-i_x-3-\frac{v_x}{4}+I = 0$$

$$I = i_x+3+\frac{v_x}{4} = i_x+3+\frac{(-4)}{4} = i_x+2 \qquad \text{...(i)}$$

Apply KVL around the outer loop,

$$-50 + 10i_x + 5I + 4i_x = 0$$

$$5I = 50 - 14i_x$$

⇒ $$I = \frac{50-14i_x}{5} \qquad \text{...(ii)}$$

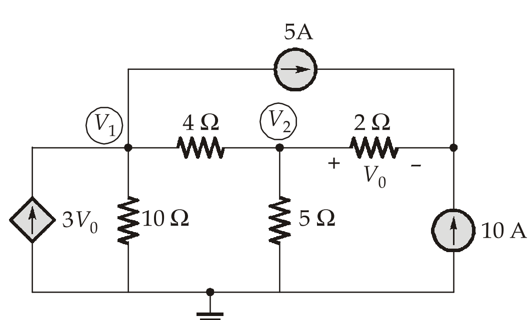
On equating equations (i) and (ii),

$$i_x + 2 = \frac{50-14i_x}{5}$$

$$5i_x + 10 = 50 - 14i_x$$

⇒ $$i_x = \frac{40}{19} = 2.105 \text{ A}$$

2. (b)



Here, 'V_1' and 'V_2' are two node voltages.
The current through 2 Ω resistor

$$= 5 + 10 = 15 \text{ A}$$

∴ The voltage, $V_0 = -2 \times (5 + 10) = -2 \times (15) = -30$ V

Apply KCL at node V_1,

$$-3V_0 + \frac{V_1}{10} + 5 + \frac{V_1 - V_2}{4} = 0$$

$$V_1\left(\frac{1}{10} + \frac{1}{4}\right) - \frac{V_2}{4} = -5 + (3 \times -30)$$

$$0.35V_1 - 0.25V_2 = -95 \qquad \text{...(i)}$$

Apply KCL at node V_2,

$$\frac{V_2 - V_1}{4} + \frac{V_2}{5} + \frac{V_0}{2} = 0$$

$$\frac{-V_1}{4} + V_2\left(\frac{1}{4} + \frac{1}{5}\right) = \frac{30}{2}$$

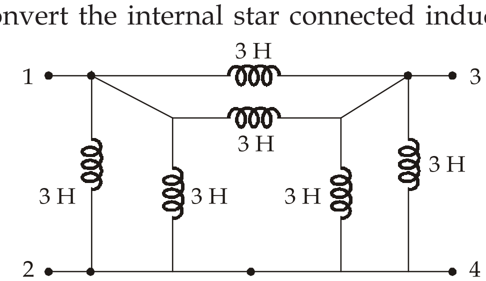
$$-0.25\,V_1 + 0.45V_2 = 15 \qquad \text{...(ii)}$$

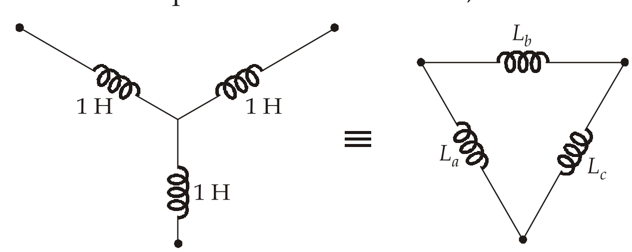
Equations (i) and (ii) can be expressed in the matrix form as

$$\begin{bmatrix} 0.35 & -0.25 \\ -0.25 & 0.45 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -95 \\ 15 \end{bmatrix}$$

3. (d)

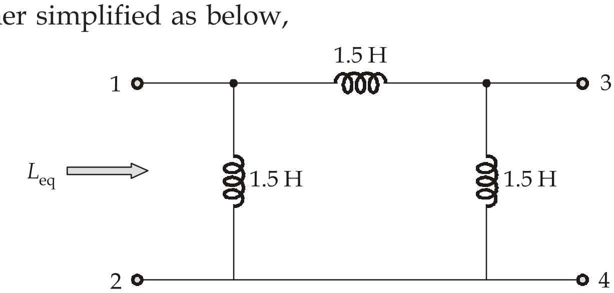
Convert the internal star connected inductances to an equivalent delta network,





$$L_a = L_b = L_c = 1 + 1 + \frac{1 \times 1}{1} = 3 \text{ H}$$

The circuit can be further simplified as below,



$$L_{eq} = 1.5 \,\|\, [1.5 + 1.5]$$

$$= 1.5 \,\|\, 3$$

$$= 1 \text{ H}$$

4. (b)

Given,
$$C = 100\ \mu F = 100 \times 10^{-6}\ F$$
$$W = 5\ mJ = 5 \times 10^{-3}\ J$$
$$I = 0.5\ A$$

The energy stored in the capacitance is given by

$$W = \frac{Q^2}{2C}$$

The charge,
$$Q = \sqrt{2CW}$$
$$= \sqrt{2\times100\times10^{-6}\times5\times10^{-3}}$$
$$= \sqrt{10^{-6}} = 10^{-3}$$

∴ $$Q = 10^{-3}\ \text{coulomb}$$

The time to charge the capacitor upto this level by the charging current is,

$$t = \frac{Q}{I} = \frac{10^{-3}}{0.5} = 2\times10^{-3}$$

⇒ $$t = 2\ \text{msec}$$

5. (c)

Whenever an ideal voltage source and ideal current source are connected in series, the current through the combination would be same as the current source. Hence, it will behave like an ideal current source alone and if they are connected in parallel, it will behave like an ideal voltage source alone.

6. (d)

Given,
$$V_1 = 100(1 + j)\ V = 100\times\sqrt{2}\angle45°\ V$$

The current,
$$I = \frac{V_1 + V_2}{[10 \| j10]}$$

⇒ $$I = \frac{100(1+j)+100(1-j)}{\left[\dfrac{10\times j10}{10+j10}\right]}$$

⇒ $$I = \frac{200(10+j10)}{(100j)} = \frac{2\times10(1+j)}{j}$$

⇒ $$I = \frac{20\sqrt{2}\angle45°}{\angle90°}$$

⇒ $$I = 20\sqrt{2}\angle-45°\ A$$

Phase angle of the current I with respect to the voltage V_1 is

$$= \angle-45° - \angle45°$$
$$= \angle-90°$$

7. (c)

For parallel circuit,

$$Y = G + j(B_C - B_L)$$

where, $$G = \frac{1}{R}, B_L = \frac{1}{X_L}, B_C = \frac{1}{X_C}$$

$\Rightarrow$ $$Y = \frac{1}{2} + j\left(\frac{1}{10}\right) - j\left(\frac{1}{5}\right)$$

$$= 0.5 + j(0.1 - 0.2)$$

$$= (0.5 - j0.1) \text{ mho}$$

8. (c)

Given, $$\overline{V} = 150 \angle 30° \text{ V}$$

$$\overline{I} = 2 \angle -15° \text{ A}$$

$$f = 50 \text{ Hz}$$

$$\overline{Z} = \frac{\overline{V}}{\overline{I}} = \frac{150\angle 30°}{2\angle -15°} = 75\angle 45°\ \Omega$$

$\Rightarrow$ Power factor angle, $\phi = 45°$

Power loss, $P = VI \cos\phi$

$$= 150 \times 2 \times \cos 45°$$

$$= 150 \times 2 \times \frac{1}{\sqrt{2}}$$

$$= 150 \times \sqrt{2} = 212.1 \text{ W}$$

9. (d)

The total admittance of the circuit is,

$$Y_T = Y_1 + Y_2$$

$$= \left[\frac{1}{R_L + j10}\right] + \left[\frac{1}{4 - j5}\right]$$

$$= \left[\frac{1}{R_L + j10} \times \frac{R_L - j10}{R_L - j10}\right] + \left[\frac{1}{4 - j5} \times \frac{4 + j5}{4 + j5}\right]$$

$$= \frac{R_L - j10}{R_L^2 + 100} + \frac{4 + j5}{41}$$

$$= \left[\frac{R_L}{R_L^2 + 100} + \frac{4}{41}\right] + j\left[\frac{5}{41} - \frac{10}{R_L^2 + 100}\right]$$

At resonance, the admittance is minimum and is real. Equating the imaginary part of admittance to zero, we get

$$\frac{5}{41} = \frac{10}{R_L^2 + 100}$$

$\Rightarrow$ $$5R_L^2 + 500 = 410$$

$$5R_L^2 = -90$$

$$R_L^2 = -18$$

$$\Rightarrow \quad R_L = \sqrt{-18} = j\sqrt{18} \quad \rightarrow \quad \text{Not a real value}$$

∴ There can't be any real value of resistance 'R_L' for which the circuit is in resonance.

10. (d)

Here, at resonance, $X_L = X_C$

Since L and C are in series, the current through L is identical to the current through C.

Now, current through L (or C) is given by

$$I = \frac{V}{X_L} = \frac{V}{2\pi f_r L}; \qquad [f_r = \text{Resonant frequency}]$$

$$= \frac{V}{2\pi\left[\frac{1}{2\pi\sqrt{LC}}\right]L} = \frac{V}{\sqrt{\frac{L}{C}}}$$

$$\Rightarrow \quad I = V\sqrt{\frac{C}{L}}\ \text{A}$$

11. (a)

Power, $P = I^2R$

$$\Rightarrow \quad R = \frac{P}{I^2} = \frac{250}{(1)^2} = 250\ \Omega$$

For a series RLC circuit, Q-factor, $Q = \frac{\omega_0 L}{R} = \frac{2\pi f_0 L}{R}$

$$\Rightarrow \quad L = \frac{QR}{2\pi f_0} = \frac{5\times250}{2\pi\times1000} = 0.2\ \text{H}$$

12. (c)

Given,
$$R = 10\ \Omega$$
$$L = 60\ \text{mH}$$
$$\omega = 100\ \text{rad/sec}$$
$$\phi = 45°$$

Since power factor angle is leading, $X_C > X_L$.

Thus,
$$\tan\phi = \frac{X_C - X_L}{R}$$

$$\tan\phi = \frac{\left(\frac{1}{\omega C}\right) - \omega L}{R}$$

$$\tan 45° = \frac{1-\omega^2 LC}{R\omega C} = 1$$

$$\therefore \quad 1 - \omega^2 LC = R\omega C$$

$$1 - [100^2 \times 60 \times 10^{-3} \times C] = 10 \times 100 \times C$$

$$1 = [1000 + 600]C$$

$$\Rightarrow \quad C = \frac{1}{1600} = 625\ \mu F$$

13. (c)

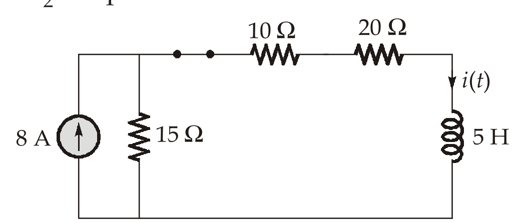
We need to consider the three time intervals, $t \le 0$, $0 \le t \le 2$, and $t \ge 2$ separately.

For $t < 0$: S_1 and S_2 are open, so $i = 0$.

Since the inductor current cannot change instantly,

$$i(0^-) = i(0^+) = i(0) = 0$$

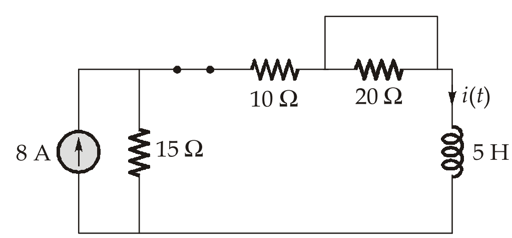
For $0 \le t \le 2$: S_1 is closed and S_2 is open.



$$R_{th} = 15 + 10 + 20 = 45\ \Omega$$

$$\tau = \frac{L}{R_{th}} = \frac{5}{45} = \frac{1}{9}$$

For $t \ge 2$:



$$R_{th} = 15 + 10 = 25\ \Omega$$

$$\tau = \frac{L}{R_{th}} = \frac{5}{25} = \frac{1}{5}$$

14. (c)

For $t > 0$, the characteristic equation of the system can be obtained using KVL as

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$$

The roots of the characteristic equation are given by

$$s = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}$$

A. $R = 2\ \Omega$, $L = \frac{1}{2}$ H, $C = 1$ F (For $t \ge 0$)

$$\alpha = \frac{R}{2L} = \frac{2}{2 \times \frac{1}{2}} = 2$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\frac{1}{2}\times 1}} = 1.414$$

$$\alpha > \omega_0 \Rightarrow \text{Overdamped response}$$

$\therefore$ $$i(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}$$

B. $\mathbf{R = 2\ \Omega, L = 1\ H, C = 1\ F}$

$$\alpha = \frac{R}{2L} = \frac{2}{2\times 1} = 1$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{1\times 1}} = 1$$

$$\alpha = \omega_0 \Rightarrow \text{Critically damped response}$$

$\therefore$ $$i(t) = e^{-\alpha t}(A_1 + A_2 t)$$

C. $\mathbf{R = 2\ \Omega, L = 5\ H, C = 1\ F}$

$$\alpha = \frac{R}{2L} = \frac{2}{2\times 5} = 0.2$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{5\times 1}} = 0.447$$

$$\alpha < \omega_0 \Rightarrow \text{Underdamped response}$$

$\therefore$ $$i(t) = e^{-\alpha t}(A_1 \cos \omega_d t + A_2 \sin \omega_d t)$$

where, $$\omega_d = \sqrt{\omega_0^2 - \alpha^2}$$

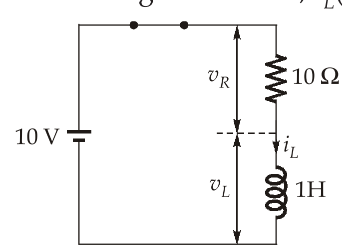
15. (b)

For $t < 0$, the circuit is source free R-L circuit.

$\Rightarrow$ $$i_L(0^-) = 0 \text{ A}$$

For $t \geq 0$:

Since the inductor doesn't allow sudden change in current, $i_L(0^-) = i_L(0^+) = 0$ A.



The inductor current is,

$$i_L(t) = i_L(\infty) + [i_L(0^+) - i_L(\infty)]e^{-t/\tau} \quad \text{...(i)}$$

Time constant, $\tau = \frac{L}{R} = \frac{1}{10}$

At steady state, inductor acts as short circuit. Thus,

$$i_L(\infty) = \frac{10}{10} = 1 \text{ A}$$

$\therefore$ From equation (i), $$i_L(t) = 1 + [0 - 1]e^{-t/(1/10)} = 1 - e^{-10t} \text{ A}$$

$$\Rightarrow \qquad v_L(t) = \frac{L di_L(t)}{dt} = (1)\times\frac{d}{dt}(1-e^{-10t}) = -(-10)e^{-10t} = 10e^{-10t} \text{ V}$$

$$v_R(t) = 10 \times i_L(t) = 10(1 - e^{-10t}) \text{ V}$$

When
$$v_R(t) = v_L(t),$$
$$10(1 - e^{-10t}) = 10e^{-10t}$$
$$1 - e^{-10t} = e^{-10t}$$
$$\frac{1}{2} = e^{-10t}$$
$$\Rightarrow \qquad t = -0.1\ln\left(\frac{1}{2}\right)$$

16. (c)

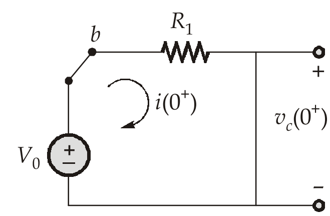
17. (d)

At $t = 0^-$, the network has attained steady-state condition. Hence, the capacitor acts as an open circuit.

$$\Rightarrow \qquad V_{c_1}(0^-) = V_0$$

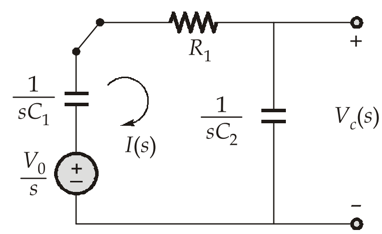
At $t = 0^+$:

$$v_c(0^+) = 0$$
$$i(0^+) = \frac{V_0}{R_1}$$



For $t \geq 0$:

The s-domain equivalent of the given circuit can be drawn as below,



Apply KVL around the loop,

$$-\frac{V_0}{s} + \left(\frac{1}{sC_1} + R_1 + \frac{1}{sC_2}\right) I(s) = 0$$

$$I(s) = \frac{\left(\frac{V_0}{s}\right)}{\left(\frac{1}{sC_1} + R_1 + \frac{1}{sC_2}\right)} = \frac{V_0}{s}\left[\frac{1}{\frac{R_1}{s}\left(s + \frac{1}{R_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\right)}\right]$$

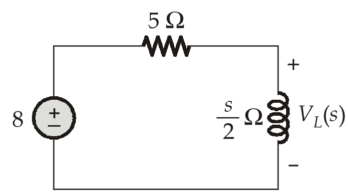
$$I(s) = \frac{V_0}{R_1}\left[\frac{1}{s + \frac{1}{R_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)}\right]$$

Take inverse Laplace transform on both sides,

$$i(t) = \frac{V_0}{R_1} e^{-\frac{1}{R_1}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)t} \; ; \; t \geq 0$$

18. (d)

The s-domain equivalent of the given circuit is,



$$V_L(s) = \frac{8\left(\frac{s}{2}\right)}{5+\left(\frac{s}{2}\right)} = \frac{\frac{8}{2}\times s}{\frac{1}{2}(s+10)} = \frac{8s}{(s+10)}$$

$$\Rightarrow \quad V_L(s) = 8\left[\frac{s+10-10}{s+10}\right] = 8\left[1-\frac{10}{s+10}\right]$$

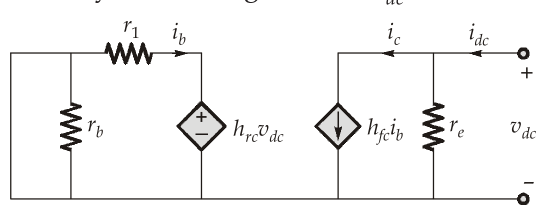
Taking inverse Laplace transform on both sides,

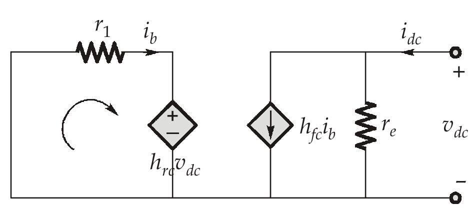
$$v_L(t) = 8[\delta(t) - 10e^{-10t}]; \quad t \geq 0$$

19. (b)

As per maximum power transfer theorem, the maximum power will be transferred to r_L when $r_L = R_{Th}$.

To find R_{Th}: Let 'r_L' be replaced by a dc voltage source v_{dc} while the source V_s is deactivated.





Apply KVL to input loop,

$$i_b r_1 + h_{rc}\, v_{dc} = 0$$

$$\Rightarrow \quad i_b = \frac{-h_{rc} v_{dc}}{r_1}$$

From the above circuit,
$$i_{dc} = \frac{v_{dc}}{r_e} + h_{fc}\, i_b$$

$$\Rightarrow \qquad i_{dc} = \frac{v_{dc}}{r_e} + h_{fc}\left(\frac{-h_{rc}v_{dc}}{r_1}\right)$$

$$= v_{dc}\left[\frac{1}{r_e} - \frac{h_{fc}h_{rc}}{r_1}\right]$$

$$\Rightarrow \qquad R_{\text{th}} = \frac{v_{dc}}{i_{dc}} = \frac{1}{\left[\frac{1}{r_e} - \frac{h_{fc}h_{rc}}{r_1}\right]} = r_L \quad \text{(for maximum power transfer)}$$

20. (d)

In AC circuits, for maximum power transfer,

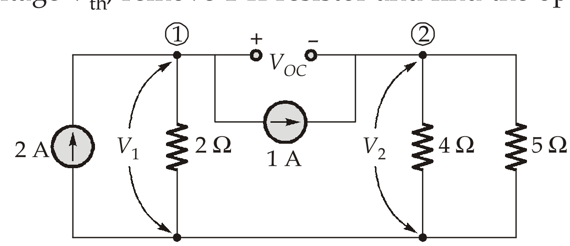
- $Z_L = Z_{th}^*$; if the impedance has variable reactive component. Thus, for circuit A, $Z_l = Z_s^*$ and for circuit D, $X_l - X_s$.
- $Z_L = |Z_{\text{th}}|$; if the impedance has only variable resistive component.

Thus, for circuit C, $\qquad R_l = \sqrt{R_s^2 + (X_s + X_l)^2}$

and for circuit B, $\qquad R_l = |Z_s| = \sqrt{R_s^2 + X_s^2}$

21. (b)

To find the Thevenin's voltage V_{th}, remove 1 Ω resistor and find the open circuit voltage across it.



Apply KCL at node (1),

$$-2 + \frac{V_1}{2} + 1 = 0$$

$$\frac{V_1}{2} = 2 - 1$$

$$\Rightarrow \qquad V_1 = 2\text{ V}$$

Apply KCL at node (2),

$$-1 + \frac{V_2}{4} + \frac{V_2}{5} = 0$$

$$\Rightarrow \qquad V_2 = \left(\frac{1}{\frac{9}{20}}\right) = \frac{20}{9}\text{ V}$$

$$\therefore \qquad V_{\text{Th}} = V_{OC} = V_1 - V_2 = 2 - \frac{20}{9} = \frac{18-20}{9} = \frac{-2}{9}\text{ V}$$

22. (b)

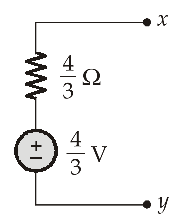
Using Millman's theorem,

$$V = \frac{V_1G_1 + V_2G_2 + V_3G_3}{G_1 + G_2 + G_3}$$

Here, V_1 = –4 V, V_2 = –2 V and V_3 = 10 V. Thus,

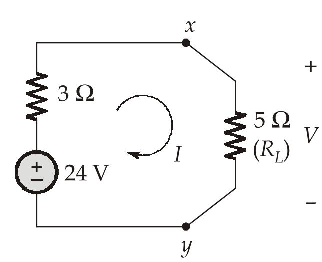
$$V = \frac{-4\times\frac{1}{4} - 2\times\frac{1}{4} + 10\times\frac{1}{4}}{\frac{1}{4}+\frac{1}{4}+\frac{1}{4}} = \frac{-1-\frac{1}{2}+\frac{5}{2}}{\frac{3}{4}} = \frac{4}{3}\text{ V}$$

$$R = \frac{1}{G} = \frac{1}{G_1+G_2+G_3} = \frac{1}{\frac{1}{4}+\frac{1}{4}+\frac{1}{4}} = \frac{4}{3}\ \Omega$$



Millman's equivalent

23. (d)



$$I = \frac{24}{3+5} = 3\text{ A}$$

$\Rightarrow$ $$V = I \times 5 = 3 \times 5 = 15\text{ V}$$

Substitution theorem, in its simplest form tells that for branch equivalence, the terminal voltage and current must be same.

For option (d), the voltage across *x*-*y* is not equal to 15 V. Hence, option (d) is the correct answer.

24. (d)

A. Series-Parallel Connection: The resultant *h*-parameter matrix is the sum of *h*-parameter matrices of each individual two-port networks.

B. Parallel-Series Connection: The resultant *g*-parameter matrix is the sum of *g*-parameter matrices of each individual two-port networks.

C. Parallel Connection: The resultant *y*-parameter matrix for parallel connected networks is the sum of *y* matrices of each individual two-port networks.

D. Series Connection: The resultant *z*-parameter matrix for the series-connected networks is the sum of *z* matrices of each individual two-port networks.

25. (d)

Time domain analysis becomes complex when the system has special input functions and more inductors and capacitors.

26. (b)

The transmission parameters are called, specifically,

A = Open-circuit voltage ratio.

B = Negative short-circuit transfer impedance.

C = Open-circuit transfer admittance.

D = Negative short-circuit current ratio.

We have, $$B = \frac{\Delta z}{z_{21}}$$

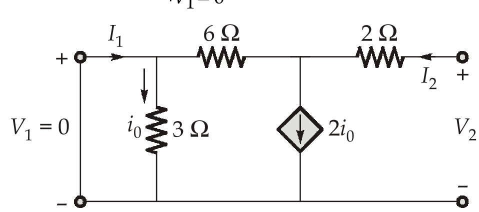
$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} 6 & 4 \\ 4 & 6 \end{bmatrix} \Rightarrow \Delta_z = \begin{vmatrix} 6 & 4 \\ 4 & 6 \end{vmatrix} = 36 - 16 = 20$$

$$\Rightarrow \quad B = \frac{20}{4} = 5\,\Omega$$

27. (c)

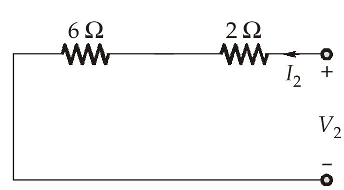
"y_{22}" is called short-circuit output admittance given as,

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}$$



Due to short-circuit, "i_0" becomes zero, thus the dependent source can be open circuited.

The simplified circuit is,



$$\therefore \quad y_{22} = \frac{I_2}{V_2} = \frac{1}{6+2} = \frac{1}{8} = 0.125\,\text{S}$$

28. (c)

In a complete graph, every pair of distinct vertices is connected by a unique edge. The exact number of edges required to make a graph complete with 'n' nodes are $^nC_2 = \frac{n(n-1)}{2}$

The given graph has '5' nodes.

$\Rightarrow$ Number of edges in complete graph $= \frac{n(n-1)}{2} = \frac{5(5-1)}{2} = 10$

29. (d)

The tree is a connected sub-graph of the given graph, which contains all the nodes of the graph. However, there should not be any loop in the sub-graph. Thus, if a network has 'n' nodes, there are $(n - 1)$ branches in the tree and there exists only one path between any pair of nodes. Therefore, all the given statements are correct.

30. (b)

The transpose of the given matrix is given by,

$$[A^T] = \begin{bmatrix} -1 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & 1 \end{bmatrix}$$

The number of possible trees is,

$$T = \text{Det}\{[A] \cdot [A^T]\}$$

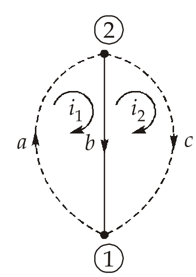
$$= \text{Det}\left\{\begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 \\ 1 & 0 & 0 & -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} -1 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & 1 \end{bmatrix}\right\}$$

$$= \text{Det}\begin{bmatrix} 2 & 0 & -1 \\ 0 & 2 & -1 \\ -1 & -1 & 3 \end{bmatrix}$$

$$= 2[6 - 1] - 1[0 + 2] = 10 - 2 = 8$$

31. (d)

By considering branch 'b' as tree, there are two fundamental loops $\{a, b\}$ and $\{b, c\}$

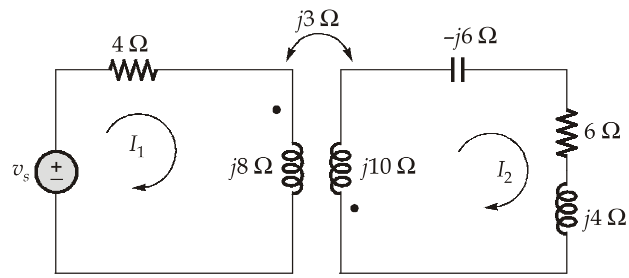


where, i_1 and i_2 are fundamental loop currents (orientation is governed by the link in it).

The tie-set matrix is,

$$[B] = \begin{matrix} & \begin{matrix} a & b & c \end{matrix} \\ \begin{matrix} i_1 \\ i_2 \end{matrix} & \begin{bmatrix} 1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}_{2\times 3} \end{matrix}$$

32. (a)



Applying KVL to mesh-1,

$$-v_s + (4 + j8)I_1 + j3I_2 = 0 \quad \text{...(i)}$$

Applying KVL to mesh-2,

$$(-j6 + 6 + j4 + j10)I_2 + j3I_1 = 0$$

$$\Rightarrow \quad I_2 = \frac{-j3I_1}{6+j8} \quad \text{...(ii)}$$

Substituting equation (ii) in (i),

$$-v_s + (4+j8)I_1 + j3\left[\frac{-j3I_1}{6+j8}\right] = 0$$

$$I_1\left[4+j8+\frac{9}{6+j8}\right] = v_s$$

$$\therefore \quad Z_{\text{in}} = \frac{v_s}{I_1} = \left[4+j8+\frac{9}{6+j8}\right] = \frac{(4+j8)(6+j8)+9}{(6+j8)}$$

$$Z_{\text{in}} = \frac{24+32j+48j-64+9}{6+j8} = \left[\frac{-31+j80}{6+j8}\right]\Omega$$

33. (c)

$A \rightarrow$ Mutually adding – coils in parallel.

$B \rightarrow$ Mutually opposing – coils in parallel.

$C \rightarrow$ Mutually opposing – coils in series.

$D \rightarrow$ Mutually adding – coils in series.

For coils in series, $L_{eq} = L_1 + L_2 \pm 2M$

(+ for series aiding connection and – for series opposing connection)

For coils in parallel,

$$L_{\text{eq}} = \frac{L_1L_2 - M^2}{L_1 + L_2 \pm 2M}$$

(– for parallel aiding connection and + for parallel opposing connection)

34. (d)

Tie set matrix gives the relation between the tie set currents and branch currents. Thus, the order of B_f is $(b - n + 1) \times b$ and it's rank is $(b - n + 1)$. Further, the submatrix corresponding to twigs (B_t) is not an identity matrix and the submatrix corresponding to links (B_l) is a identity matrix of order $(b - n + 1)$.

35. (a)

$$v_L(t) = \frac{L di_L(t)}{dt}$$

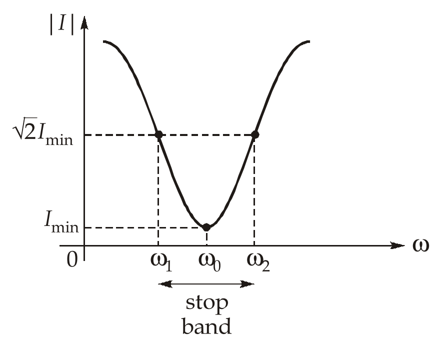
If $i_L(t) = u(t) \Rightarrow v_L(t) = L\delta(t)$
which is a sudden spike and not acceptable.

$$i_c(t) = \frac{C dv_c(t)}{dt}$$

If $v_c(t) = u(t) \Rightarrow i_c(t) = C\delta(t)$
which is a sudden spike and not acceptable.

36. (b)

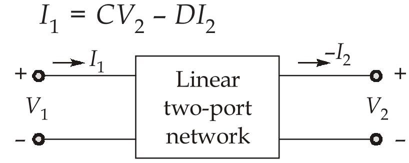
Under parallel resonance condition, the net admittance is minimum so current is also minimum, hence it acts as "rejector circuit". Thus, this phenomenon can be used in the design of band stop or band rejection filter.



At parallel resonant frequency, the currents through 'L' and 'C' components are Q-times the supply current. Hence, this circuit is considered as "current amplification circuit".

37. (a)

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2$$



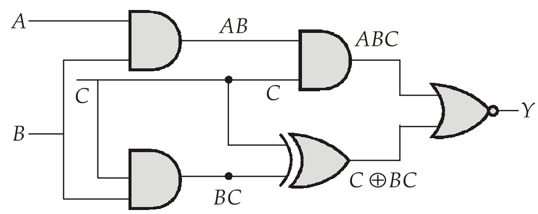
The above two-port parameters provide a measure of how a circuit transmits voltage and current from a source to a load. These parameters are useful in the analysis of transmission lines (such as cable and fiber) because they express sending-end variables (V_1 and I_1) in terms of the receiving-end variables (V_2 and $-I_2$). For this reason, these parameters are called transmission parameters, and are also known as *ABCD* parameters. These parameters are used in the design of telephone systems, microwave networks, and radars.

38. (a)

Inductors are used to store energy in the form of magnetic field when an electric current is passed through it. In inductor, once we give input, it should be continuous in order to flow current continuously. Hence, compare to inductor, capacitor is used as memory element because it retains the charged voltage upto some extent of time.

Section B : Digital Circuits

39. **(d)**



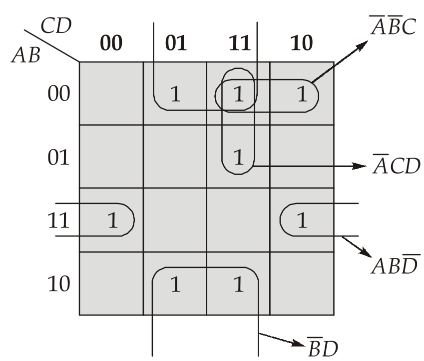
$$C \oplus BC = \bar{C}BC + \overline{BC}C$$
$$= 0 + \bar{B}C$$

$\therefore$ output $Y = \overline{ABC + \bar{B}C} = \overline{ABC} \cdot \overline{\bar{B}C}$

$$= (\bar{A} + \bar{B} + \bar{C}) \cdot (B + \bar{C})$$
$$= \bar{A}B + \bar{A}\bar{C} + \bar{B}B + \bar{B}\bar{C} + B\bar{C} + \bar{C}$$
$$= \bar{A}B + \bar{C}(\bar{A} + \bar{B} + B + 1)$$
$$Y = \bar{C} + \bar{A}B$$

40. **(d)**

Redrawing the given K-map in the correct order,



$\therefore$ $F = \bar{B}D + \bar{A}\bar{B}C + \bar{A}CD + AB\bar{D}$

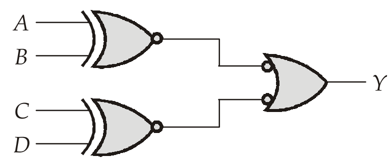
41. **(a)**

To avoid glitches in the output, in the master-slave D flip flop, the master latch captures the input data on one edge of the clock (i.e. the positive edge), and the slave latch transfers that data to the output on the opposite edge (i.e. the negative edge). Hence, it works as a negative edge triggered D flip-flop. Therefore, statements 1 and 2 are correct.

42. **(d)**

Given, $F = A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D$

$$= A\bar{B}[C\bar{D} + \bar{C}D] + \bar{A}B[C\bar{D} + \bar{C}D]$$
$$= [A\bar{B} + \bar{A}B][C\bar{D} + \bar{C}D]$$
$$= (A \oplus B)(C \oplus D)$$
$$= \overline{(A \odot B) + (C \odot D)}$$



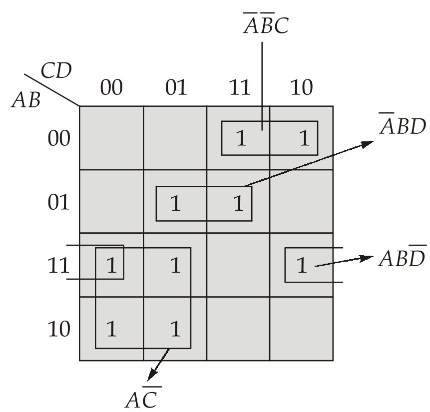
43. (a)

$$Y = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

$$Y = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB(\overline{CD})$$

$$Y = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB\bar{C} + AB\bar{D}$$

By using 4-Variable K-map:



$$\text{Output } Y = A\bar{C} + AB\bar{D} + \bar{A}BD + \bar{A}\bar{B}C$$

44. (d)

$$F = \overline{A(B+C)+(C+D)(B+E)}$$

$$= \overline{AB+AC+BC+CE+BD+DE}$$

$$F = \overline{B(A+D)+C(A+B+E)+DE}$$

45. (b)

Clk	Inputs				Outputs	
	J_0	K_0	J_1	K_1	Q_0	Q_1
–	1	1	0	1	0	0
1	1	1	1	1	1	0
2	0	1	0	1	0	1
3	1	1	0	1	0	0
4	1	1	1	1	1	0

Hence, the counter counts in the sequence 00 $\rightarrow$ 10 $\rightarrow$ 01.

If $Q_1Q_0 = 11$, then $J_0 = 0$, $J_1 = 1$

After applying clock pulse,

output, $Q_0 = 0$; $Q_1 = 0$

So, option (b) is correct.

46. (d)

The given circuit A is a 1-bit comparator circuit.

X	Y	**Outputs**	$X < Y$	$X > Y$	$X = Y$
0	0	Y_0	0	0	1
0	1	Y_1	1	0	0
1	0	Y_2	0	1	0
1	1	Y_3	0	0	1

Since the output of logic gate is 1 , whenever $X = Y$ i.e. either $Y_0 = 1$ or $Y_1 = 1$. Thus, the logic gate is an OR Gate. We have,

$$S = \bar{X}\bar{Y} + XY = X \odot Y$$

∴ Output of 2 × 1 MUX,

$$F = \bar{S} I_0 + S I_1$$
$$= (\overline{X \odot Y})X\bar{Y} + (X \odot Y)\cdot 1$$
$$= (\bar{X}Y + X\bar{Y})X\bar{Y} + \bar{X}\bar{Y} + XY$$
$$= X\bar{Y} + \bar{X}\bar{Y} + XY$$
$$= X + \bar{X}\bar{Y}$$

∴ $$= X + \bar{Y}$$

47. (b)

Given, clock frequency, $f_{\text{clk}} = 10$ MHz,

The cascade counter is MOD-4000 counter.

(∵ — MOD-5 — MOD-8 — MOD-10 — MOD-10 —)

∴ output lowest frequency, $f_{0L} = \dfrac{f_{clk}}{4000}$

$$f_{0L} = \frac{10 \times 10^6}{4000} = 2.5 \text{ kHz}$$

48. (b)

The truth table for above functionality,

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

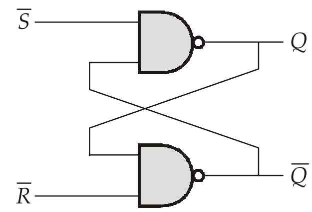
$$Y = \bar{A}\bar{B} + A\bar{B} + AB = \bar{B} + AB = A + \bar{B}$$

49. (a)

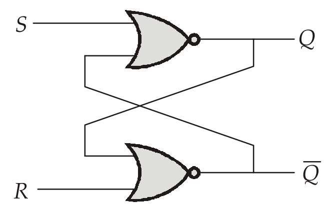
TTL logic family has leakage current in the HIGH state and has assymmetric output drive; they can sink much more current in the low state than they can source in the high state.

50. (b)

A latch is a bistable multivibrator with two stable states. Active-low input SR latch uses NAND gates. Here, when the S input is active low, the latch is set and when R input is active low, the latch is reset.



Active high input SR latch uses NOR gates. Here, when the S input is active high, the latch is set and when R input is active high, the latch is reset.



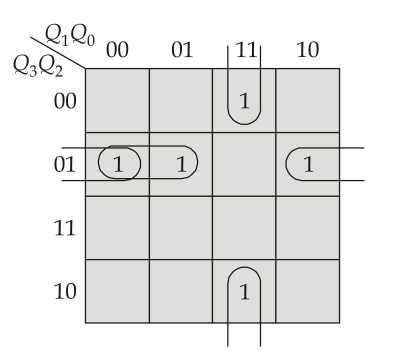
The regenerative feedback is the characteristic of all latches and flip-flops i.e. the outputs are fed back into the inputs.

51. (c)

State-Table of the given sequential circuit can be written as below,

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	$D_2 = Q_2^+$
0	0	1	1	0	1	0	0	1
0	1	0	0	0	1	0	1	1
0	1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0	0
1	0	1	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1
1	1	0	0	0	0	1	1	0

By using 4-variable K-map:



$$D_2 = \overline{Q}_2Q_1Q_0 + \overline{Q}_3Q_2\overline{Q}_0 + \overline{Q}_3Q_2\overline{Q}_1$$

$$= \overline{Q}_3Q_2(\overline{Q}_0 + \overline{Q}_1) + \overline{Q}_2Q_1Q_0$$

52. (d)

We have, $A = \bar{S}_0 I_0 + S_0 I_1$

where, $I_0 = Y; I_1 = 0$

$\therefore$ $A = \bar{0} Y + 0 \cdot 0$

$A = Y$

We have, $B = \bar{S}_1 I_0 + S_1 I_1$

$= \bar{0} \cdot X + 0 \cdot 0$

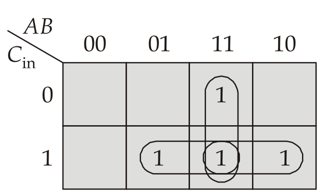
$\therefore$ $B = X$

53. (a)

Truth table:

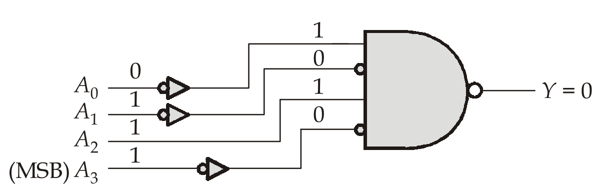
C_{in}	A	B	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$\therefore$ C_{out}:



$\therefore$ $C_{out} = AB + C_{in}B + AC_{in}$

54. (c)



The output of NAND Gate is zero when all the inputs are at logic '1'.

$\therefore$ $A_3 A_2 A_1 A_0 = 0111$

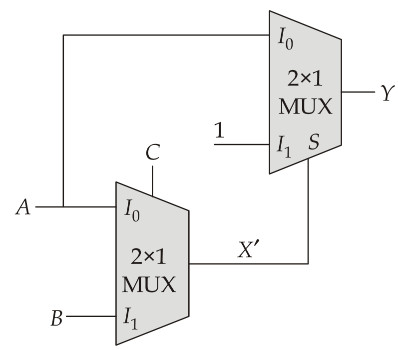
55. (d)

Inputs to flip flops, $J_2 = \bar{Q}_0; J_1 = Q_2; J_0 = Q_1; K_2 = Q_0; K_1 = \bar{Q}_1; K_0 = \bar{Q}_2$

Initial State			Inputs						Next State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	1	0	0	1	0	1	1	0	0
1	0	0	1	0	1	1	0	0	1	1	0
1	1	0	1	0	1	0	1	0	1	1	1
1	1	1	0	1	1	0	1	0	0	1	1

56. (b)

The given circuit can be modified as,



$$Y = \bar{S}I_0 + SI_1 = \bar{S}A + S(1)$$

where $$S = X' = A\bar{C} + BC$$

∴ $$Y = \overline{A\bar{C} + BC}(A) + (A\bar{C} + BC)$$

$$= \left[\overline{A\bar{C}} \cdot \overline{BC}\right]A + A\bar{C} + BC$$

$$= (\bar{A} + C)(\bar{B} + \bar{C})A + A\bar{C} + BC$$

$$= (\bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}C)A + A\bar{C} + BC$$

$$= A\bar{B}C + A\bar{C} + BC$$

$$= C(A\bar{B} + B) + A\bar{C} = C(A + B) + A\bar{C}$$

$$Y = A(C + \bar{C}) + BC = A + BC$$

57. (d)

For a dual slope *ADC*, $$V_a = V_R \cdot \frac{N}{2^n}$$

where N : decimal equivalent of digital output; n = number of bits

∴ $$2.25 = 4 \times \frac{N}{2^4}$$

$$N = \frac{2.25 \times 2^4}{4} = 9$$

$$N = (1001)_2$$

58. (d)

Given, 8-bit DAC

$$\text{digital input} = (00110010)_2 = 50_{10}$$

For a DAC,

$$\text{output } V_0 = \text{Resolution} \times (\text{Decimal equivalent of input})$$

$$1.0 = \text{Resolution} \times 50$$

$$\therefore \quad R = \frac{1.0}{50} = 20 \text{ mV}$$

The largest output value occurs for digital input of $11111111_2 = 255_{10}$

$$\therefore \quad V_{out} = R \times (255)_{10} = 20 \times 10^{-3} \times 255 = 5.10 \text{ V}$$

59. (b)

For $T = 0$, the propagation delay is

$$t_{pd}(\text{MUX-1}) + t_{pd}(\text{MUX-2}) = 1 \text{ ns} + 1 \text{ ns}$$
$$= 2 \text{ ns delay}$$

for $T = 1$, the path followed is

$t_{pd}(\text{inv}) + t_{pd}(\text{MUX-1}) + t_{pd}(\text{MUX-2}) + t_{pd}(\text{inv}) = 0.5 + 1 \text{ ns} + 0.5 \text{ ns} + 1 \text{ ns} = 3 \text{ ns}$

$\therefore$ maximum propagation delay = 3 nsec

60. (c)

The truth table of the full subtractor is as below,

A	B	B_{in}	Difference	Borrow (B_{out})
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The inputs of MUX can be obtained as,

Select Lines (AB)	Borrow (B_{out})	Input Lines
00	B_{in}	$I_0 = B_{in}$
01	1	$I_1 = 1$
10	0	$I_2 = 0$
11	B_{in}	$I_3 = B_{in}$

Hence, option (c) is correct.

61. (d)

$$\text{output function, } F = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$$

Here,

$$I_0 = 0;\ I_1 = 0,\ I_2 = 0;\ I_3 = 1$$

$$\therefore \quad F = AB$$

62. (c)

Given, 5-bit DAC,

$$V_{out} = 0.2 \text{ V for input } 00001.$$

which is equivalent to as the weight of the LSB.

Thus, the weights of the other bits must be, +0.4 V, +0.8 V, +1.6 V and +3.2 V

For digital input 11011, the value of V_{out} will be 3.2 V + 1.6 V + 0.4 V + 0.2 V

$$= 5.4 \text{ V}$$

63. (a)

Given,
$$Y = 1$$
$$S = 0$$

$$\therefore \quad Y = \bar{S} \cdot I_0 + SI_1$$

Initially, $Y = 1$. For $S = 0$; $I_0 = 1$; $I_1 = 0$. Thus,

$$Y = \bar{0}.1 + 0.1 = 1$$

Thus, the output remains constant at 1.

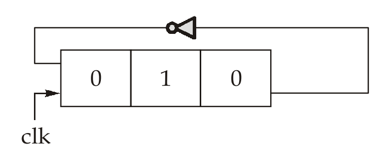
64. (a)

clk	J	K	Q_{JK}	Q_D	D
XX	–	–	0	1	0
1	1	1	1	0	1
2	1	1	0	1	0
3	1	1	1	0	1

$\therefore$ After 3rd clock cycle, $Q_D \ Q_{JK} = 01$

65. (a)

A 3-bit Johnson counter with initial state 010 is shown below,



clk	Count
XX	$0\ 1\ 0 = 2_{10}$
1	$1\ 0\ 1 = 5_{10}$
2	$0\ 1\ 0 = 2_{10}$
3	$1\ 0\ 1 = 5_{10}$
	⋮

The counting sequence of the counter is $2 \to 5 \to 2 \to 5 \to 2$

66. (a)

Let $f'(X, Y)$ be the output of pull down logic,

$$\therefore \quad f'(X, Y) = \overline{XY + \bar{X}\bar{Y}}$$

$$\therefore \quad f(X, Y) = \overline{\overline{XY + \bar{X}\bar{Y}}} = XY + \bar{X}\bar{Y}$$

Hence, the circuit implements XNOR Gate.

67. (c)

$$\text{Output function, } F = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$$
$$= \bar{A}\bar{B}\bar{C} + \bar{A}BD + A\bar{B}(0) + AB(\bar{C} + D)$$
$$= \bar{A}\bar{B}\bar{C} + \bar{A}BD + AB\bar{C} + ABD$$

AB \ CD	00	01	11	10
00	1	1		
01		1	1	
11	1	1	1	
10				

$\therefore$ $$F = \Sigma m(0, 1, 5, 7, 12, 13, 15)$$

68. (a)

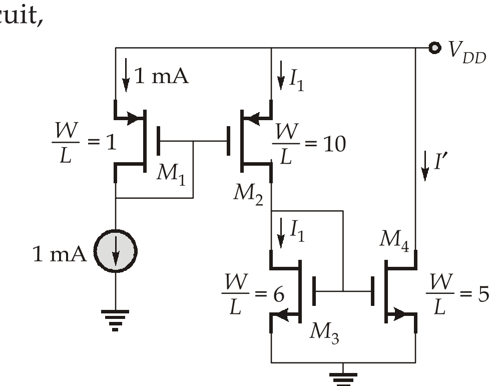
The truth table for the circuit can be drawn as below:

X	Y	Z	
0	0	0	pnp is ON (closed switch) and diode of OFF
0	1	0	pnp is ON and diode is ON
1	0	1	pnp is OFF (open switch) and diode is OFF
1	1	1	pnp is OFF and diode is ON

$\therefore$ $$Z = X\bar{Y} + XY = X$$

69. (c)

By redrawing the given circuit,



We know that, for nMOSFET, $I_D \propto \dfrac{W}{L}$ [for same V_{GS}]

We have, $V_{GS}(M_1) = V_{GS}(M_2)$, thus $I_1 = \dfrac{\left(\frac{W}{L} = 10\right)}{\left(\frac{W}{L} = 1\right)} \times 1\text{ mA} = 10\text{ mA}$

Considering M_3 and M_4, $I' = I_1 \times \dfrac{5}{6} = 10\text{ mA} \times \dfrac{5}{6} = 8.33\text{ mA}$

70. (b)

For adding 16-bit numbers,

At LSB, Half adder is used and for remaining 15-bits, 15 full-adders are used.

∴ To add 16-bit numbers, 1 half-adder and 15 full-adders are required.

71. (a)

$$(74)_x = (35)_y$$

$$7x + 4 = 3y + 5$$

$$\Rightarrow \quad 7x - 3y = 1$$

The bases $x = 4$ and $y = 9$ satisfy the above relation,

$$7 \times 4 - 3 \times 9 = 28 - 27 = 1$$

72. (d)

Given Boolean expression,

$$[z' + wx' + w'y + wy'z + w'y'z]'$$

$$= [z' + wx' + w'y + wy'z + w'y'z]'$$

$$= [z' + wx' + w'y + y'z(w + w')]'$$

$$= [z' + wx' + w'y + y'z]'$$

$$= [z' + wx' + w'y + y'z]'$$

$$= [(z' + y'z) + wx' + w'y]'$$

$$= [z' + (y' + w'y) + wx']'$$

$$= [z' + y' + w' + wx']'$$

$$= [z' + y' + x' + w']'$$

$$= [(wxyz)']' = wxyz$$

73. (d)

$$f = y(\overline{x} + z) = \overline{x}y + yz$$

x \ yz	00	01	11	10
0			1	1
1			1	

Thus, $f = \Sigma m(2, 3, 7)$

74. (b)

Given, $(0.1010)_2 = (0.6x5y)_{10}$

$$(0.1010)_2 = 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4}$$
$$= 0.5 + 0 + 0.125 + 0$$
$$= (0.6250)_{10}$$
$$= (0.6x5y)_{10}$$

On comparing, $x = 2;\ y = 0$

$\therefore$ $x + y = 2 + 0 = 2$

75. (a)

Fan-out defines the maximum number of logic inputs that a single output of a logic gate can drive reliably.

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