CLASS TEST

S.No. : 01JP_CS_10062024

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COMPUTER SCIENCE & IT

Computer Organization

Duration : 1:00 hr. **Maximum Marks : 50**

Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q. No. 1 to Q. No. 10 carry 1 mark each

Q.1 Consider the following statements with respect to control unit.

S_1 : Operating speed of vertical microprogramming is higher than that of horizontal microprogramming.

S_2 : Horizontal microprogramming needs signal decoders as like vertical microprogramming.

Which of the following option in correct?

(a) Both S_1 and S_2 are correct
(b) Only S_1 is correct
(c) Only S_2 is correct
(d) None of S_1 or S_2 is correct

Q.2 A non-pipeline processor has a clock rate 4 MHz and an average CPI of 5. An upgrade to the processor introduce 5 stage pipeline. How ever due to internal delay the clock rate of the new processor has to be reduces to 3 MHz. What is the speed-up of pipeline over non-pipeline?

(a) 3.1 (b) 3.7
(c) 3.5 (d) 4.1

Q.3 Consider the following IEEE single precision floating point number shown below:

01000011110100000000000000000000

The octal equivalent of above number is__.

(a) 200 (b) 640
(c) 416 (d) 320

Q.4 A PC relative mode branch instruction is 5 B long. The address of the instruction in decimal is 238715. The branch target address if the signed displacement is –32 is _____.

(a) 238752 (b) 238715
(c) 238688 (d) 238720

Q.5 Consider a hypothetical control unit that supports 5 groups of mutually exclusive control signals. Also assume that group-1 and group-2 are using horizontal micro-programming where as group-3, 4 and 5 are using vertical micro-programming. The total number of bits used for control words are ____ .

Groups	G_1	G_2	G_3	G_4	G_5
Control signals	3	9	6	13	10

(a) 23 (b) 12
(c) 11 (d) 14

Q.6 Consider the following statements:

S_1 : More than one word are put in one cache block to reduce the miss penalty.

S_2 : Virtual memory increases the degree of multiprogramming.

S_3 : Increasing the RAM of a computer typically improves performance because virtual memory increase.

How many of the above statements are correct?

(a) Only S_1 and S_3
(b) Only S_1 and S_2
(c) Only S_2
(d) All S_1, S_2 and S_3

Q.7 A cache block has 64 kbyte. The main memory has latency 64 μsec and bandwidth 1 GBps. The total time required to fetch the entire cache block from the main memory (in μsec, $1G = 10^9$) is

(a) 256 μsec
(b) 128 μsec
(c) 32 μsec
(d) 64 μsec

Q.8 Consider a small 2-way set associative cache memory, consisting of 4 blocks. For choosing the block to be replaced, use LRU scheme. Consider that block address 4 and 2 are already there in cache. The number of cache misses for the following sequence of block addresses 4, 6, 8, 16, 2, 2, 4 are _____.

(a) 5 (b) 6
(c) 4 (d) 7

Q.9 Consider a 32 bit microprocessor that has on chip 32 K byte 4 way set associative cache. Block size of cache is two 32 bit words. The set number (in decimal) to which the word from memory location FAFEEBE1 wrapped _____.

(a) 385 (b) 420
(c) 380 (d) 400

Q.10 Consider the following statements:

S_1 : 3 control signals are needed for memory data register.

S_2 : The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same block.

Which of the following option is correct ?

(a) Only S_1 is true
(b) Only S_2 is true
(c) Both S_1 and S_2 are true
(d) Neither of S_1 or S_2 is true

Q. No. 11 to Q. No. 30 carry 2 marks each

Q.11. Consider 1GHz clock frequency processor, uses different operand access modes shown below:

Operand Access Mode	Frequency (%)
Register	20
Immediate	20
Memory Indirect	40
Auto Indexed	20

Assume that 8 cycle consumed for memory reference, 4 cycles consumed for arithmetic computation and 0 cycles consumed when the operand is in register instruction itself. What is the average operand fetch rate (in million words/sec) of the processor?

(a) 117.45 M words/sec
(b) 113.63 M words/sec
(c) 217.45 M words/sec
(d) 316.45 M words/sec

Q.12 Consider the cache memory which is 30 times faster than main memory and it can be uses 90% of the total time. What is the speedup gain by cache memory?

(a) 7.33
(b) 7.46
(c) 7.69
(d) 7.52

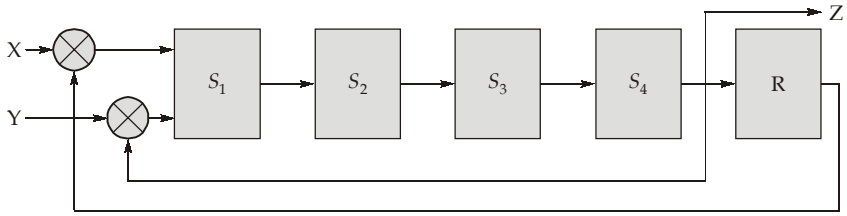
Q.13 Consider the following program segment:

	Instruction	Meaning	Instruction size (in word)
I_1	Load r_0, 300	$r_0 \leftarrow [300]$	2
I_2	MOV r_1, 5000	$r_1 \leftarrow$ Mem [5000]	2
I_3	MOV r_2, (r_1)	$r_2 \leftarrow$ Mem [r_1]	1
I_4	Add r_0, r_2	$r_0 \leftarrow r_0 + r_2$	1
I_5	MOV, 6000, r_0	Mem [6000] $\leftarrow r_0$	2
I_6	HALT	Machine Halts	1

Consider that the memory is byte addressable with word size 16 bits and the program has been loaded starting from memory location $(2000)_{10}$. The return address will be saved in the stack, if an interrupt occurs while the CPU has been halted after executing the HALT instruction is _____.

(a) 2000
(b) 2016
(c) 2008
(d) 2018

Q.14 Consider a multiplier pipeline with 5 stages which consist of input lines X and Y and output line Z. The pipeline has a register R as its output, where the temporary result can be stored and feed back to S_1 at a later point in time. The inputs X and Y are multiplexed with the outputs R and Z.



Assume that elements of vector A are fed in to the pipeline through input X, one element per cycle. The minimum number of clock cycles required to compute the product of an element vector.

The following code is running on a above pipeline with operand forwarding.

	Instruction	**Meaning**	
I_1 :	Load ACC, R	ACC ← (R)	{R = A_i}
I_2 :	Inc, R	R ← (R) + 1	
I_3 :	Mul ACC, R	ACC ← (ACC) × (R)	
I_4 :	Store R, ACC	R ← (ACC)	

How many cycles required to compute the program _____.

(a) 6 (b) 8
(c) 7 (d) 5

Q.15 A 4-way set associative cache memory consists of 128 blocks. The main memory consist of 32768 memory blocks and each block contain 512 eight bit words. Find how many bits are needed to represent TAG, SET and WORD field respectively?

(a) 5, 9, 10 (b) 10, 6, 8
(c) 10, 9, 5 (d) 10, 5, 9

Q.16 Suppose that a processor has access to three levels of memory. Level 1 contain 2000 words and has an access time of 0.02 msec. Level 2 contain 10,000 words and has an access time of 0.2 msec. Level 3 contains 20,000 words and has an access time of 2 msec. Assume that if a word to be accessed is in level 1, then processor access it directly. If it is in level 2 the word is first transferred to L_1 and then accessed by the processor. Similarly for L_3 the word is transferred to L_2 then to L_1 and then accessed. The hit ratio for level 1 is 0.65 and for level 2 is 0.45. The average access time (in μsec) is _____.

(a) 482 (b) 472
(c) 475 (d) 480

Q.17 A DMA module is transferring characters to memory using cycle stealing mode, from a device which is transmitting at a rate of 19200 bps. The rate at which processor is fetching the instruction is 2 million instructions per second (2 MIPS). Due to DMA, CPU slowed down by _____

(a) 0.11 (b) 0.15
(c) 0.5 (d) 416.6

Q.18 Consider the following statement. Out of the statements choose the one which best characterize computers that use memory mapped I/O.

(a) the computer provides special instruction for manipulating I/O port.
(b) I/O ports are placed at address on bus and as accessed just like other memory location.
(c) to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.
(d) ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

Q.19 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Programmed IO
B. Interrupt driven IO
C. Direct memory access

List-II

1. On I/O command issued by the processor, the processor busy-waits for the operation to be completed.
2. After issuing an I/O command, processor continues to execute subsequent instructions, and is interrupted by the concerned module, when latter has completed its work.
3. Processor send a request for the transfer of a block of data to the concerned module and is interrupted when the entire block has been transferred.

Which of the following code is correct?

Codes:

	A	B	C
(a)	1	3	2
(b)	1	2	3
(c)	2	1	3
(d)	1	3	2

Q.20 A 4-way set associative cache has lines of 32-byte and a total cache size of 16 KB. Which of the 256 MB main memory block is mapped on to the set '50' of the cache memory?

(a) $(CFED09B)_{16}$ (b) $(FB3D64C)_{16}$
(c) $(FDE1400B)_{16}$ (d) $(CFED109B)_{16}$

Q.21 Consider the following sequence of instructions executed on a 5 stage pipelined procesor. Data dependency is resolved by operand forwarding techniques. MOV instruction output present in 4^{th} stage and ALU operation output present in 3^{rd} stage.

I_1 : MOV R_0, M[300]
I_2 : SUB R_0, R_1
I_3 : ADD R_2, R_1
I_4 : MOV R_3, @ 200
I_5 : MUL R_2, R_3

What is the number of cycles required to complete the program? (Assume each stage takes 1 cycle time)

(a) 8 (b) 9
(c) 10 (d) 11

Q.22 Consider a 5 GHz clock frequency processor used to execute the following program segment on a pipelined processor.

Instruction	Size (in words)	Meaning
I_1 : MOV r_0, [300]	3	$r_0 \leftarrow$ M[300]
I_2 : MOV r_1, @ 400	4	$r_1 \leftarrow$ M[[400]]
I_3 : MUL r_0, r_1	2	$r_0 \leftarrow r_0 * r_1$
I_4 : MOV r_1, @ 500	4	$r_2 \leftarrow$ M[[500]]
I_5 : DIV r_0, r_2	1	$r_0 \leftarrow r_0 / r_2$

Each memory references and ALU operation consumes 3 cycles and 1 cycles respectively. The total time required to complete the program execution is

(a) 8.4 ns (b) 7.33 ns
(c) 15.62 ns (d) 11.8 ns

Q.23 Consider the following statements:

S_1 : Hardwired control unit design is not suitable in design and testing places.
S_2 : Horizontal micro programmed control unit design is implemented using sum of product expression on a flip-flops.
S_3 : Vertical micro programmed control unit allows high degree of the parallelism with respect to horizontal μ-program control unit.
S_4 : In the control unit design control signals are represented in a encoding format/ decoding format/SOP format.

Which of the following statements are true?
(a) S_1 only S_2 only
(b) S_1 and S_4, S_3 only
(c) S_1 and S_4 only
(d) S_1, S_2 and S_4

Q.24 Consider the following statements:
(i) To increment or decrement its value Program Counter (PC) does not require ALU operation.
(ii) Memory conflict in structural dependency can be minimized using operand forwarding technique.
(iii) Delayed branch technique is used to optimize the control dependency.

Which of the following is true?
(a) (i) - false, (ii) - true, (iii) - true
(b) (i) - false, (ii) - false, (iii) - true
(c) (i) - true, (ii) - false, (iii) - false
(d) (i) - true, (ii) - false, (iii) - true

Q.25 Consider 5 stage pipeline which allows overlapping of all the instructions except memory based instructions. Penality of the memory based instruction is 3 cycles. In the program 40% memory instructions are present, among them 60% are optimized. What is the average instruction execution time? (Assume the pipeline cycle time as 8 ns)
(a) 9.76 ns (b) 11.84 ns
(c) 14.84 ns (d) 13.76 ns

Q.26 Consider the machine with a byte addressable main memory of 2^{16} byte, block size of 16 byte and a 2 way set associative mapped cache having 2^{10} lines. Suppose there are two bytes in main memory i.e. first byte address $[\text{E } 01 \text{ F}]_{16}$ and second byte address $[\text{E } 208]_{16}$ respectively then the difference of the set value (in decimal) between given two bytes i.e. (SET value of second byte – SET value of 1st byte) is _____.
(a) 34 (b) 32
(c) 33 (d) 31

Q.27 Consider the following program segment:

	Instruction	Meaning	Size (words)
I_1	LOAD r_0, 500	$r_0 \leftarrow [500]$	2
I_2	MOV r_1, r_0	$r_1 \leftarrow [r_0]$	1
I_3	ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_4	INC r_0	$r_0 \leftarrow r_0 + 1$	1
I_5	INC r_1	$r_1 \leftarrow r_1 + 1$	1
I_6	ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_7	Store r_1, r_0	$M[(r_1)] \leftarrow r_0$	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location $(3001)_{10}$ onwards. The value of PC at the end of execution of above program is _____.
(a) 3009
(b) 3010
(c) 3006
(d) 3008

Q.28 Consider two different implementations of the same instruction set architecture, P_1 and P_2. Processor P_1 runs on a clock rate of 1.5 GHz and P_2 runs on 2.5 GHz. There are four classes of instructions A, B, C and D. The CPI's of each implementation are given in the following table.

	Class A	Class B	Class C	Class D
CPI's of P_1	1	2	3	4
CPI's of P_2	2	2	2	2
Frequency	10%	10%	50%	30%

Given a program with 10^6 instructions divided into 4 classes according to the frequencies in the above table. Choose the correct statement from the following.
(a) P_1 is faster than P_2
(b) P_2 is faster than P_1
(c) P_1 is same as P_2
(d) None of these

Q.29 Consider the following floating point format.

Sign(s)	Exponent (E)	Mantissa (M)
1 bit	8 bits	23 bits

The decimal number (– 48.625) has following hexadecimal representation with normalization and rounding off

(a) C4228000
(b) 42428000
(c) C2428000
(d) None of these

Q.30 A 1-address machine and 2-address machine executes the instructions to compute X = (A+ B × C)/ (D – E × F). The instructions available for 1-address machine is LOAD, STORE, ADD, SUB, MUL, and DIV. The instructions available for 2-address machine is MOV, ADD, SUB, MUL and DIV. How many extra instructions required by 1-address machine compared to 2-address machine?

(a) 2 (b) 5
(c) 8 (d) 11

■■■■

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Date of Test : 10/06/2024

ANSWER KEY ➤

1.	(d)	7.	(b)	13.	(b)	19.	(b)	25.	(b)
2.	(b)	8.	(a)	14.	(c)	20.	(b)	26.	(d)
3.	(b)	9.	(c)	15.	(d)	21.	(d)	27.	(b)
4.	(c)	10.	(d)	16.	(c)	22.	(d)	28.	(b)
5.	(a)	11.	(b)	17.	(a)	23.	(d)	29.	(c)
6.	(c)	12.	(c)	18.	(b)	24.	(d)	30.	(a)

DETAILED EXPLANATIONS

1. (d)

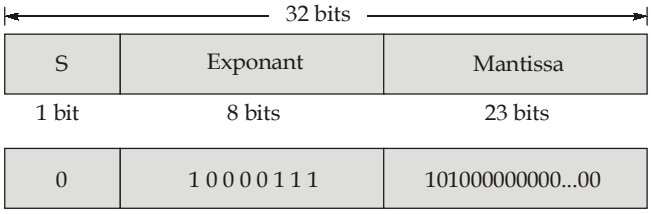
- Since, vertical microprogram encode the control signals hence a signal decoder is needed which decrease the operational speed of vertical micro-programming in comparison with horizontal micro-programming.
- Since, the control signal bits under horizontal microprogram control unit are not encoded. Hence no signal decoder is needed.

2. (b)

$$ET_{\text{non-pipe}} = \text{Average CPI} \times \text{Cycle time (non-pipe)}$$
$$= 5 \times 0.25\ \mu\text{sec} = 1.25\ \mu\text{sec}$$
$$ET_{\text{pipe}} = \text{Average CPI}_{\text{pipe}} \times \text{Cycle time (pipe)}$$
$$= 1 \times 0.33\ \mu\text{sec} = 0.33\ \mu\text{sec}$$
$$\text{Speed-up} = \frac{ET_{\text{non-pipe}}}{ET_{\text{pipe}}} = \frac{1.25}{0.33} = 3.78 \approx 3.7$$

3. (b)

Format of single precision floating point is



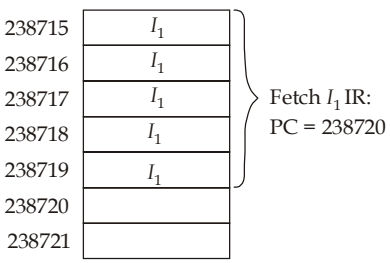
$$\text{Value} = 1.M \times 2^{E-127}$$
$$= 1.1010 \times 2^{135\ -\ 127}$$
$$= (1.1010)_2 \times 2^8$$
$$= 1.625 \times 2^8$$
$$= (416)_{10}$$

Octal representation

8	416	
8	52	0
	6	4

Octal representation is (640).

4. (c)



$$\text{Effective address} = \text{PC} + \text{Relative value}$$
$$= 238720 + (-32) = 238688$$

5. **(a)**

Given:

Group-1 and 2 are using horizontal micro-programming,

Hence, total bits are:

$$3 + 9 = 12$$

Group-3, 4 and 5 are using vertical micro-programming,

Hence, total bits are:

$$\lceil \log_2 6 \rceil + \lceil \log_2 13 \rceil + \lceil \log_2 10 \rceil = 3 + 4 + 4 = 11$$

Total bits for control word = 12 + 11 = 23 bits

6. **(c)**

- More than one word are put in one cache block to explicit in the spatial locality of reference.
- By the help of virtual memory, programs can exceed from the size of primary memory, hence increases the degree of multi programming.
- Increasing RAM will result in fewer page faults.

Hence only S_2 is the correct statement.

7. **(b)**

For 1 second it take 10^9 byte

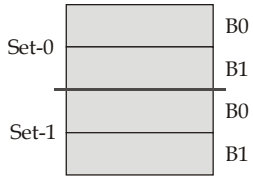
So for 64 kbyte it takes = $\frac{64k}{10^9}$ = 64 μsec

Main memory latency = 64 μsec

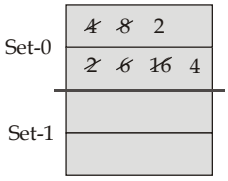
Total time required to fetch = 64 μsec + 64 μsec = 128 μsec

8. **(a)**

Cache will be divided as,

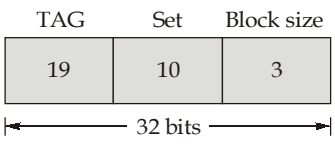


Since block addresses 4 and 2 are already there,



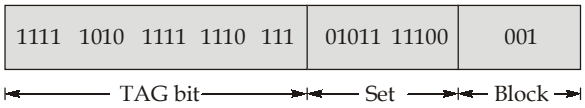
Total number of misses= 5

9. **(c)**



$$\text{Number of lines} = \frac{32 \times 2^{10}\text{B}}{2^3\text{B}} = 2^{12}$$

$$\text{Number of set} = \frac{2^{12}}{4\,\text{Way}} = 2^{10}$$

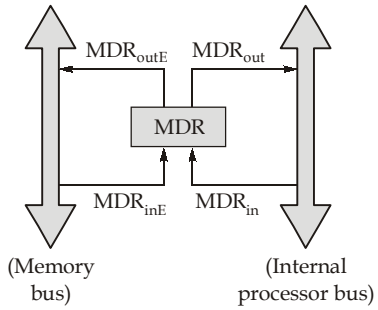


Set = 0101111100 = 380

10. (d)

Considering each statement:

S_1 : 4-control signals are needed for each data register.



MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

S_2 : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

11. (b)

Average cycles/instruction = {(0.2 × 0) + (0.2 × 0) + (0.4 × 16) + (0.2 × 12)}
= {6.4 + 2.4} = 8.8 cycles

So, average time = 8.8 nsec

1 operand requires 8.8 nsec

Number of operands fetched in 1 sec

$$\text{Number of operands} = \frac{1\ \text{sec}}{8.8\ \text{nsec}} = 0.113636 \times 10^9\ \text{operand/sec}$$

Operand fetch rate = 113.636 million words/sec

12. (c)

$$\text{Speedup (S)} = \frac{1}{(1-\text{Cache \% used}) + \left[\frac{\text{Cache \% used}}{\text{Speedup using cache}}\right]}$$

$$= \frac{1}{(1-F)+\left(\frac{F}{S}\right)} = \frac{1}{(1-0.9)+\left(\frac{0.9}{30}\right)} = \frac{1}{(0.1)+\left(\frac{0.9}{30}\right)}$$

$$= \frac{30}{3.9} = 7.69$$

13. (b)

	Instruction	Instruction size	Location
I_1	Load r_0, 300	2 word	2000-2003
I_2	MOV r_1, 5000	2 word	2004-2007
I_3	MOV r_2, (r_1)	1 word	2008-2009
I_4	Add r_0, r_2	1 word	2010-2011
I_5	MOV, 6000, r_0	2 word	2012-2015
I_6	HALT	1 word	2016-2017

$\therefore$ Since 1 word is of 2 bytes.

If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address 2016 is saved in the stack.

14. (c)

The minimum number of clock cycles can be obtained by writing its assembly code. The process in obtaining the outputs Z and R from input line X or Y via the same manner, such that the codes are not much different except there is a line code to execute store command when using input line X. The code is as follows:

Instruction	Meaning	
I_1 : Load ACC, R	ACC $\leftarrow$ (R)	{R = A_i}
I_2 : Inc, R	R $\leftarrow$ (R) + 1	
I_3 : Mul ACC, R	ACC $\leftarrow$ (ACC) $\times$ (R)	
I_4 : Store R, ACC	R $\leftarrow$ (ACC)	

Constructing the table:

	1	2	3	4	5	6	7
I_1	F	D	E	W			
I_2		F	D	E	W		
I_3			F	D	E	W	
I_4				F	D	E	W

So, the minimum clock cycles required to complete one process is 7 clock cycles.

15. (d)

Main memory size = 32768 blocks

1 block = 512 words

= 32768 × 512 words = $2^{15} \times 2^9 = 2^{24}$ words

Main memory takes 24 bits.

Block size = 512 words = 2^9 words

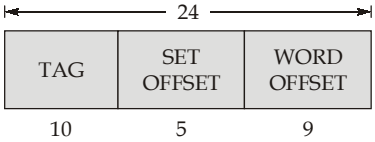
Number of bits for block size = 9 bits.

Number of blocks in set associative = 128

Number of blocks in one set = 4

$$\text{Number of sets in cache} = \frac{128}{4} = 32 = 2^5$$

Number of bits in set offset = 5 bits



Number of TAG bits = 24 – (9 + 5) = 10 bits

16. (c)

$$\begin{aligned} T_{avg} &= h_1 t_1 + (1 - h_1)h_2 (t_2 + t_1) + (1 - h_1)(1 - h_2)(t_3 + t_2 + t_1) \\ &= 0.65 \times 0.02 + 0.35 \times 0.45 \times 0.22 + 0.35 \times 0.55 \times 2.22 \\ &= 0.013 + 0.03465 + 0.42735 \\ &= 0.475 = 475\ \mu\text{sec} \end{aligned}$$

17. (a)

DMA transfer character at rate of 19200 bpsec

8 bit = 1 character

So, 192000 bit = 2400 character

So, 1 sec = 2400 character

$$1 \text{ character (X)} = \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec}$$

$$= 416.6\ \mu\text{sec}$$

Processor fetch rate is 2 MIPS

1 MIPS = 1 sec

$$1 \text{ Instruction (Y)} = \frac{1}{2 \times 10^6} = 0.5\ \mu\text{sec}$$

$$\% \text{ slow down using DMA} = \left(\frac{Y}{X + Y}\right) \times 100$$

$$= \left(\frac{0.5}{416.6 + 0.5}\right) \times 100 = 0.11\%$$

18. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

19. (b)

Programmed I/O: Processor issues an IO command, on behalf of a processor, to an IO module; that process then busy-waits for the operation to be completed before proceeding.

Interrupt driven I/O: The processor issues an IO command on behalf of a process, continues to execute subsequent instruction, and is interrupted by the IO module when the latter has completed its work.

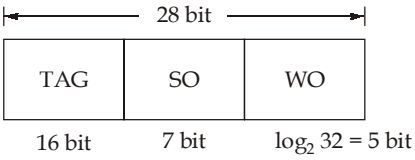
Direct memory access: A DMA module controls the exchange of data between main memory and IO module.

20. (b)

$$\text{Number of lines} = \frac{16\text{ KB}}{32\text{ B}} = \frac{2^{14}}{2^5} = 2^9$$

$$\text{Number of sets} = \frac{2^9}{2^2} = 2^7$$

Physical address size = 256 MB = 28 bits



Total set will be from 0 to 127 (using 7 bits).
In option (b)

$$(FB3D64C)_{16} = F\ B\ 3\ D\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 0\ C$$

16 bit TAG | 7 bit set | 5 bit WO

It's decimal value is 50

Hence option (b) is correct.

21. (d)

	1	2	3	4	5	6	7	8	9	10	11
I_1	IF	ID	EX	MM	WB						
I_2		IF	ID	ID	EX	MM	WB				
I_3			IF	IF	ID	EX	MM	WB			
I_4					IF	ID	EX	MM	WB		
I_5						IF	ID	ID	EX	MM	WB

Total 11 cycles are required.

22. (d)

IF	ID	OF	PD and WB
I_1 : 1 memory reference	2 memory reference	1 memory reference	–
I_2 : 1 memory reference	3 memory reference	2 memory reference	–
I_3 : 1 memory reference	1 memory reference	–	1 ALU operation
I_4 : 1 memory reference	3 memory reference	2 memory reference	–
I_5 : 1 memory reference	–	–	1 ALU operation

Total Execution Time = (Number of memory reference × 3 cycles + Number of ALU operation × 1 cycles) × cycle time

$$= (19 \times 3 + 2 \times 1) \times \frac{1}{5\text{ GHz}} = \frac{59}{5}\text{ ns} = 11.8\text{ ns}$$

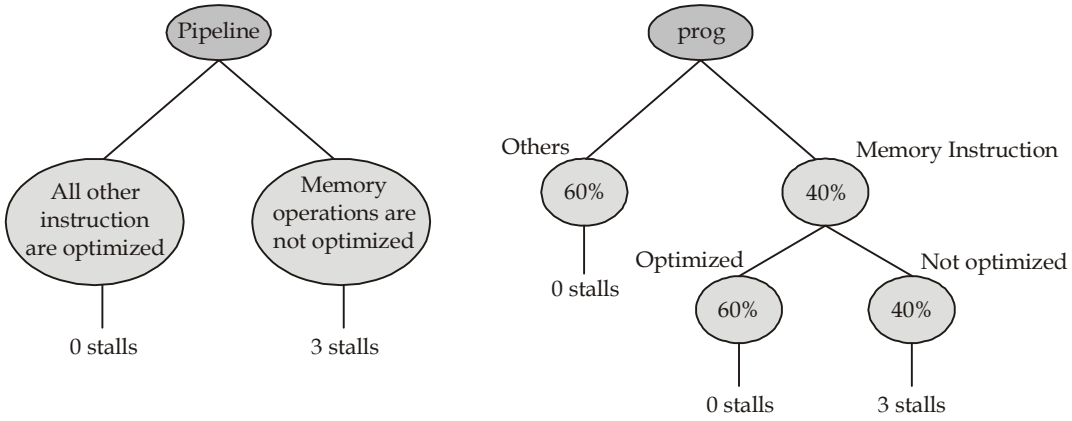
23. (d)

- Hardwired control unit design is not suitable in design and testing places because small modification change the working of whole system. So, we have to design again.
- Horizontal control unit design is implemented using sum of product expression on a flip-flops.
- Vertical micro programmed control unit allows low degree of the parallelism, whereas horizontal micro programmed control unit allows high degree of the parallelism.
- In the control unit design control signals are represented in a encoding format/decoding format/SOP format.

24. (d)

(i) is true, it is logically done.
(ii) is false, structural dependency resolved using re-naming.
(iii) Delayed branch re-arranges code to reduce control dependency.

25. (b)



Number of stalls/Instruction = (0.4 × 0.4 × 3) = 0.48

Average instruction ET = (1 + # stalls / Instruction) × Cycle time
= (1 + 0.48) × 8 ns = 11.84 ns

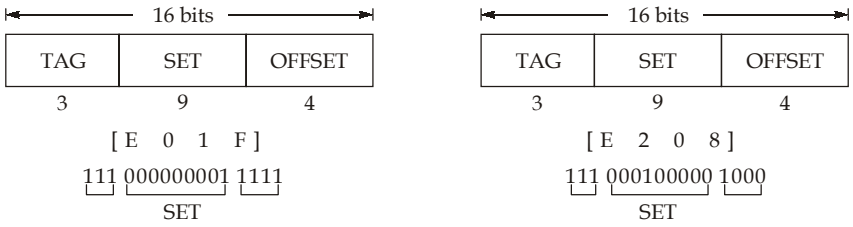
26. (d)

Block size = 16 byte = 2^4 byte = 4 bits

Blocks in main memory = 2^{10}

So number of sets = $\frac{2^{10}}{2^1} = 2^9 \Rightarrow 9$ bits

Number of bits in physical address = 2^{16} byte $\Rightarrow$ 16 bits



SET value$_1$ = 000000001 = Decimal value = $(1)_{10}$

SET value$_2$ = 000100000 = Decimal value = $(32)_{10}$

Difference = $SET_2 - SET_1$
= 32 – 1 = $(31)_{10}$

27. (b)

Word addressable storage

3001 – 3002	→	I_1
3003	→	I_2
3004	→	I_3
3005	→	I_4
3006	→	I_5
3007	→	I_6
3008 – 3009	→	I_7
3010	→	I_8

Valid program counter value after program is 3010.

28. (b)

$$P_1 \text{ CPU time} = \frac{[1 \times 0.1 + 2 \times 0.1 + 3 \times 0.5 + 4 \times 0.3]}{1.5 \times 10^9}$$

$$= 2 \times 10^{-9} \text{ sec} = 2 \text{ nsec}$$

$$P_2 \text{ CPU time} = \frac{[2 \times 0.1 + 2 \times 0.1 + 2 \times 0.5 + 2 \times 0.3]}{2.5 \times 10^9}$$

$$= 0.8 \times 10^{-9} \text{ sec} = 0.8 \text{ nsec}$$

$\therefore$ P_2 is faster than P_1 processor.

29. (c)

The decimal number is = (– 48.625)

Binary number representation of (– 48.625)

Normalization form = 1.10000101×2^5

Mantissa field is = 10000101000000000000000

Exponent field is = $5 + 127 = 132 = (10000100)_2$

Value in given format is

Sign(s)	Exponent (E)	Mantissa (M)
1	100 00100	100 00101000000000000000
	C 2	4 2 8 0 0 0

So the hexadecimal representation is $(C2428000)_{16}$.

30. (a)

$$X = (A + B \times C)/(D - E \times F)$$

1-Address Machine:

1. LOAD E
2. MUL F
3. STORE T
4. LOAD D
5. SUB T
6. STORE F
7. LOAD B
8. MUL C
9. ADD A
10. DIV T
11. STORE X

So, total 11 instruction in 1-address machine.

2-Address Machine:

1. MOV R_0, E
2. MUL R_0, F
3. MOV R_1, D
4. SUB R_1, R_0
5. MOV R_0, B
6. MUL R_0, C
7. ADD R_0, A
8. DIV R_0, R_1
9. MOV X, R_0

Total 9 instructions in 1-address machine.

So, 2 extra instruction is required in 1-address machine.

■■■■