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DIGITAL ELECTRONICS

EC-EE

Date of Test : 05/08/2024

ANSWER KEY >

- | | | | | |
|--------|---------|---------|---------|---------|
| 1. (b) | 7. (d) | 13. (b) | 19. (b) | 25. (d) |
| 2. (b) | 8. (b) | 14. (a) | 20. (d) | 26. (a) |
| 3. (d) | 9. (b) | 15. (c) | 21. (c) | 27. (c) |
| 4. (c) | 10. (d) | 16. (d) | 22. (c) | 28. (c) |
| 5. (a) | 11. (c) | 17. (b) | 23. (a) | 29. (c) |
| 6. (b) | 12. (b) | 18. (a) | 24. (c) | 30. (b) |

DETAILED EXPLANATIONS

1. (b)

Since the decoder have active low outputs, for any input the signal on corresponding data line will be low or logic zero.

For NAND gate if one or more number of inputs are low, then its output will be high.

$$\therefore F = \sum m(0, 2, 3, 6) = \prod M(1, 4, 5, 7)$$

2. (b)

$$x \oplus y = x\bar{y} + \bar{x}y = \overline{xy + \bar{x}\bar{y}}$$

Since, $xy = 0$

$$x \oplus y = \overline{0 + \bar{x}\bar{y}} = x + y$$

3. (d)

$$\begin{aligned} F &= \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + ABC = \bar{A}(\bar{B}\bar{C} + BC) + A(\bar{B}C + B\bar{C}) \\ &= \bar{A}(B \odot C) + A(B \oplus C) = \bar{A}(\overline{B \oplus C}) + A(B \oplus C) \\ &= A \odot B \oplus C \end{aligned}$$

4. (c)

$$F = A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

To determine the inputs a table is constructed as shown below:

	I_0 $\bar{A}\bar{B}$	I_1 $\bar{A}B$	I_2 $A\bar{B}$	I_3 AB
\bar{C}	0	2	4	6
C	1	3	5	7
	C	\bar{C}	\bar{C}	C

Hence,

$$I_0 = I_3 = C$$

$$I_2 = I_1 = \bar{C}$$

5. (a)

For n bit comparator,

Number of combinations for $A > B$ is

$$\frac{2^{2n} - 2^n}{2} = \frac{2^{12} - 2^6}{2} = 2016$$

6. (b)

Squaring both sides,

$$(\sqrt{41})^2 = 5^2$$

$$(41)_B = (25)_{10}$$

$$4B + 1 = 25$$

$$B = 6$$

7. (d)

$$F = \overline{\overline{AB}(CD + \overline{EF})(\overline{AB} + \overline{CD})}$$

Using Demorgan's theorem

$$\begin{aligned} F &= \overline{\overline{AB}} + \overline{(CD + \overline{EF})} + \overline{(\overline{AB} + \overline{CD})} \\ &= AB + \overline{CD} \cdot \overline{\overline{EF}} + \overline{\overline{AB}} \cdot \overline{\overline{CD}} \\ &= AB + (\overline{C} + \overline{D})(E + \overline{F}) + ABCD \\ &= AB(1 + CD) + (\overline{C} + \overline{D})(E + \overline{F}) \\ F &= AB + (\overline{C} + \overline{D}) \cdot (E + \overline{F}) \end{aligned}$$

8. (b)

Given:

$$\begin{aligned} f(A, B) &= A + B = A \cdot 1 + B \cdot 1 \\ &= A(B + \overline{B}) + B(A + \overline{A}) \\ &= AB + A\overline{B} + BA + B\overline{A} \\ &= AB + A\overline{B} + \overline{A}B \end{aligned}$$

9. (b)

Given Karnaugh map can be grouped as below

CD \ AB	00	01	11	10
00	1	1		
01	1	1		1
11	1	1		1
10	1	1		

The Karnaugh map shows four groups of 1s:

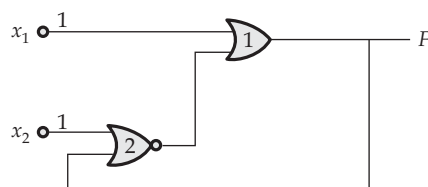
- A group of four 1s in the first two columns (AB=00, 01) for CD=00 and 01, labeled \overline{A} .
- A group of four 1s in the first two columns (AB=00, 01) for CD=00 and 11, labeled A .
- A group of two 1s in the last column (AB=10) for CD=01 and 11, labeled $D\overline{B}$.
- A group of two 1s in the last column (AB=10) for CD=11 and 10, labeled $\overline{D}B$.

10. (d)

In D flip flop when clock is high then output depends on the input otherwise remains at previous output. When clock is high and D is high, the output Q is high, if D is 0 then output is zero. Like SR flipflop, D flipflop have an invalid state when both input are 1.

11. (c)

Given arrangement



Irrespective of other input at OR gate (1) other than x_1 , F always remains 1 due to property of OR operator.

12. (b)

	Q_A	Q_B	Q_C	$D_C = Q_A \oplus Q_C$	$D_B = Q_C$	$D_A = Q_B$
	1	1	0	1	0	1
1	1	0	1	0	1	0
2	0	1	0	0	0	1
3	1	0	0	1	0	0
4	0	0	1	1	1	0
5	0	1	1	1		

After 5 clock pulse $Q_A Q_B Q_C$ will be 011.

13. (b)

$$\% \text{ resolution} = \frac{1}{2^n - 1} \times 100 = \frac{1}{2^4 - 1} \times 100\% = 6.67\%$$

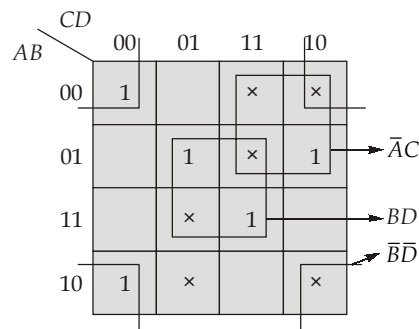
14. (a)

Minimum propagation delay = $(3 \times 50 + 75)n \text{ sec} = 225 n \text{ sec}$

Maximum additions per second = $\frac{1}{225 n \text{ sec}} = 4.44 \times 10^6 \text{ additions/sec}$

$\therefore A = 4.44$

15. (c)



The function is $BD + \bar{B}\bar{D} + \bar{A}C$

16. (d)

To create 5 bit parallel adder, we require 4-full adder plus 1 Half adder.
 For 4 full adder, we require 8 Ex-OR gates, 8 AND gates and 4-OR gates.
 and for 1 Half adder we require only 1 Ex-OR gate and one AND gate.
 Thus finally for 5-bit adder we require 9 Ex-OR gates, 9 AND gates and 4 OR gates.

17. (b)

From the given logic circuit, the expression of $Z(A, B, C)$ can be written as

$$\begin{aligned} Z &= A + \bar{A} \cdot \bar{B} \cdot \bar{C} \\ &= (A + \bar{B}\bar{C}) \quad (\because x + \bar{x}y = x + y) \\ &= A + \overline{B+C} \\ &= A \text{ OR } (B \text{ NOR } C) \end{aligned}$$

18. (a)

$$\begin{aligned}
 F &= \bar{A}\bar{B}C + A\bar{B}C + AB \\
 &= (\bar{A} + A)\bar{B}C + AB \\
 &= \bar{B}C + AB
 \end{aligned}$$

19. (b)

Given that,

$$\begin{array}{r}
 1011001111 \\
 + 1 \\
 \hline
 1011010000 \\
 \hline
 \end{array}$$

Complemented output

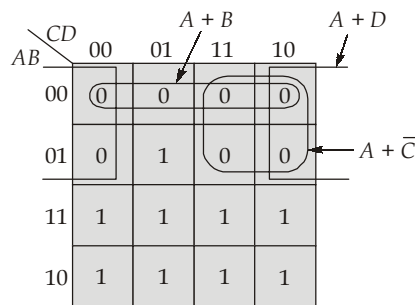
∴ No. of flip flop = 5

20. (d)

The flip-flop is connected in toggle mode. Thus, $Q_{n+1} = \bar{Q}_n$.

21. (c)

Drawing the K-map we have,



$$\begin{aligned}
 \therefore f &= \Pi M(0, 1, 2, 3, 4, 6, 7) \\
 &= (A+B)(A+\bar{C})(A+D)
 \end{aligned}$$

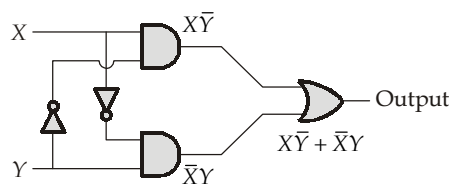
22. (c)

The excitation table of a J-K flip-flop can be given as

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

← Required excitation

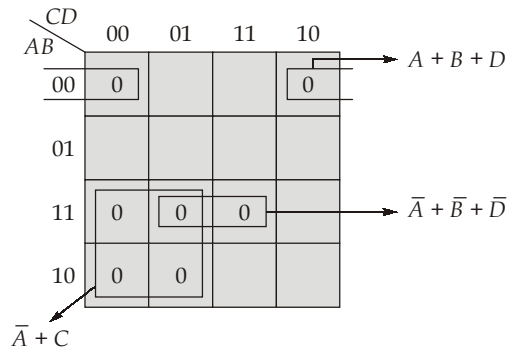
23. (a)



24. (c)

$$f(A, B, C, D) = \pi M(0, 2, 8, 9, 12, 13, 15)$$

The K-map representation is shown as,



The simplified Boolean expression is,

$$f(A, B, C, D) = (\bar{A}+C)(\bar{A}+\bar{B}+\bar{D})(A+B+D)$$

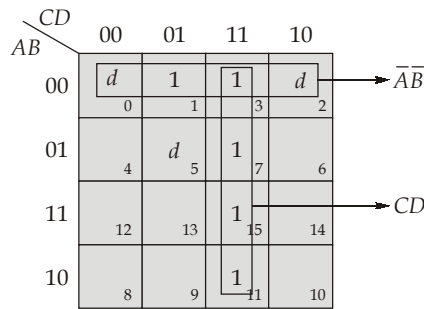
25. (d)

$$\begin{aligned} Y &= \bar{A}C(\bar{A}BD) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\ &= \bar{A}C(\bar{A}BD) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\ &= \bar{A}CA + \bar{A}C\bar{B} + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\ &= \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\ &= \bar{B}C(\bar{A}+A) + \bar{A}\bar{D}(C+B\bar{C}) \\ &= \bar{B}C + \bar{A}\bar{D}(B+C) \end{aligned}$$

[∵ $A \cdot \bar{A} = 0$]
 [∵ $x + \bar{x}y = x + y$]

26. (a)

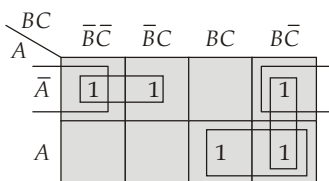
Given : $f(A, B, C, D) = \Sigma_m(1, 3, 7, 11, 15) + \Sigma_d(2, 5)$
 where d denotes don't care



The simplified expression is

$$f(A, B, C, D) = \bar{A}\bar{B} + CD$$

27. (c)



$$\text{Prime implicants} = \bar{A}\bar{B}, \bar{A}\bar{C}, AB, B\bar{C}$$

∴ Total number of prime implicants are 4.

28. (c)

Given, segment voltage = 2.8 V

Applied voltage = $V_{CC} = 5\text{ V}$, Current = 10 mA

Let current limiting resistance be R_s

$$\therefore R_s = \frac{(5 - 2.8)\text{ V}}{10\text{ mA}} = \frac{2.2}{10 \times 10^{-3}} = 220\ \Omega$$

29. (c)

$D_2(\bar{Q}_0)$	$D_1(Q_2)$	$D_0(Q_1)$	Q_2	Q_1	Q_0
1	0	0	0	0	0
1	1	0	1	0	0
1	1	1	1	1	0
0	1	1	1	1	1
0	0	1	0	1	1
0	0	0	0	0	1

$$\therefore D_2 \rightarrow \bar{Q}_0, D_1 \rightarrow Q_2, D_0 \rightarrow Q_1$$

30. (b)

