S.No.:01SK_ABCDEFGHIJKL_16924

MADE EASY
India's Best Institute for IES, GATE & PSUs

Delhi | Bhopal | Hyderabad | Jaipur | Pune | Kolkata

Web: www.madeeasy.in | **E-mail:** info@madeeasy.in | **Ph:** 011-45124612

DIGITAL LOGIC

COMPUTER SCIENCE & IT

Date of Test : 16/09/2024

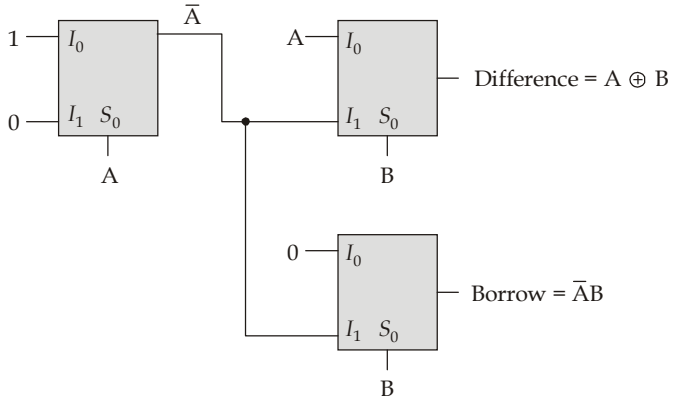
ANSWER KEY ➤

1.	(c)	7.	(c)	13.	(a)	19.	(b)	25.	(d)
2.	(a)	8.	(a)	14.	(b)	20.	(a)	26.	(b)
3.	(b)	9.	(a)	15.	(d)	21.	(d)	27.	(d)
4.	(b)	10.	(d)	16.	(d)	22.	(a)	28.	(a)
5.	(c)	11.	(c)	17.	(d)	23.	(b)	29.	(c)
6.	(c)	12.	(c)	18.	(a)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

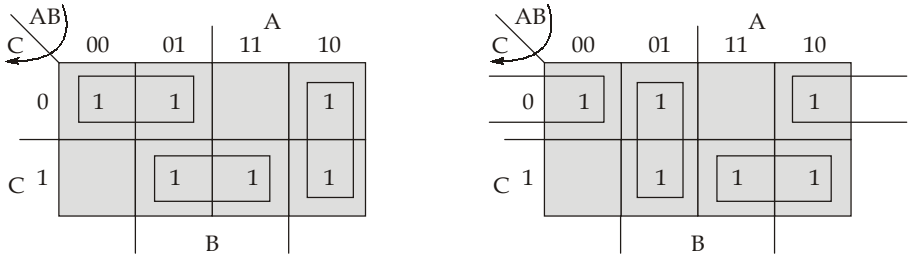
1. **(c)**

2. **(a)**



3. **(b)**

Example: $F(A, B, C) = \sum m(0, 2, 3, 4, 5, 7)$



$F(A, B, C) = \bar{A}\bar{C} + BC + \bar{A}B$ $\qquad$ $F(A, B, C) = \bar{B}\bar{C} + \bar{A}B + AC$

$F(A, B, C)$ is having cyclic PI K-map and it is having '2' minimal forms.

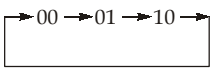
In general, based on above example when the Boolean function is having cyclic prime implicants K-map it will be having 2 minimal forms.

4. **(b)**

The truth table for the circuit is obtained below:

Present state		FF input		Next state	
Q_A	Q_B	T_A $(Q_A + Q_B)$	T_B $(\bar{Q}_A + Q_B)$	Q_A^+	Q_B^+
0	0	0	1	0	1
0	1	1	1	1	0
1	0	1	0	0	0
0	0	0	1	0	1

So, the counter counts the sequence of 3 states as



Hence, the circuit is of a MOD-3 counter.

5. **(c)**

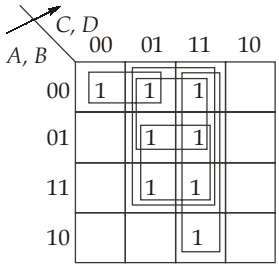
2's complement representation of –29 is 11100011.

1	0	–1
1	1	0
0	1	+1
0	0	0
0	0	0
1	0	–1
1	1	0
1	1	0

Recorded pair is : 00 – 100 + 10 – 1.

6. **(c)**

$$f(A, B, C, D) = BD + A'B'C' + ACD + B'CD$$
$$(5, 7, 13, 15)\ \ (0, 1)\ \ (11, 15)\ \ (3, 11)$$



$$f(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 11, 13, 15)$$
$$= BD + CD + A'D + A'B'C'$$

7. **(c)**

$$(11X1Y)_8 = (12C9)_{16}$$

$$001001\ X\ 001\ Y = 0001\ \ 0010\ \ 1100\ \ 1001$$

X Y

These are missing in left side. Hence $X = 3$ and $Y = 1$.

So, $X + Y = 3 + 1 = 4$

8. **(a)**

Characteristic equation for J-K flip flop:

$$Q_{n+1} = J_nQ_n' + K_n'Q_n$$

Characteristic equation for S-R flip flop:

$$Q_{n+1} = S_n + R_n'Q_n$$

9. **(a)**

Note: Clock is negative edge triggered, so when clock goes from 1 → 0 then output is changes.

CLK	Q_1 $D_1 = Z$	Q_2 $D_2 = Q_1$	Q_3 $D_3 = Q_2$	Q_4 $D_4 = Q_3$	Z
	1	0	1	0	0
1	0	1	0	1	1
2	1	0	1	0	0
3	0	1	0	1	1

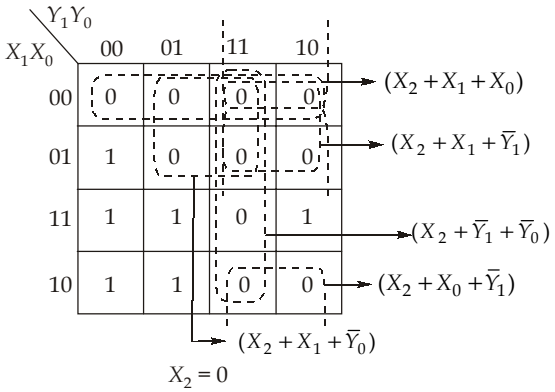
Output Z for next 3 clock cycles = 101.
Hence option (a) is correct wave form for 101.

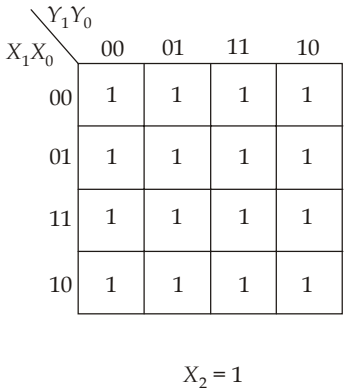
10. (d)

To generate length S we need $\log_2 S$ flip-flop.

11. (c)

Now, $X > Y$ if
(a) $X_2 = 1$
(b) $X_2 = 0$ and $X_1X_0 > Y_1Y_0$





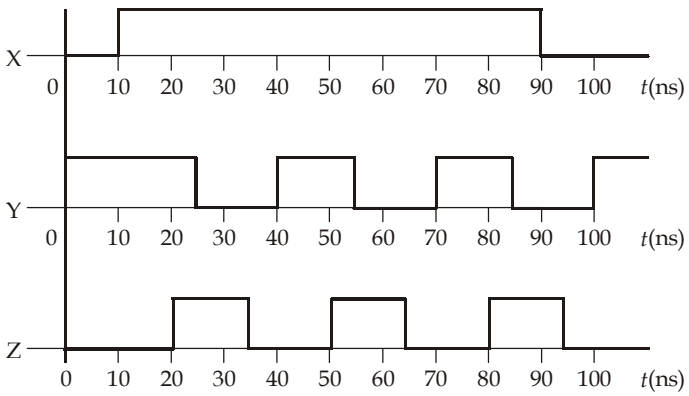
12. (c)

$$F = A(\bar{A} + B)(\bar{A} + B + \bar{C})$$
$$= (A + B\bar{B} + C\bar{C})(\bar{A} + B + C\bar{C})(\bar{A} + B + \bar{C})$$
$$= (A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + B + C)(\bar{A} + B + \bar{C})$$
$$\text{POS (F)} = M_0, M_1, M_2, M_3, M_4, M_5$$
$$= \Pi(0, 1, 2, 3, 4, 5)$$

So, $\text{SOP (F)} = (0, 1, 2, 3, 4, 5, 6, 7) - (0, 1, 2, 3, 4, 5)$
$= \Sigma(6, 7)$

So, $F = \Sigma(6, 7)$ and $F = \Pi(0, 1, 2, 3, 4, 5)$

13. (a)



Level changes at points are t = 20, 35, 50, 65, 80, 95 ns

14. (b)

$[D' + AB' + A'C + AC'D + A'C'D]'$

$= [D' + AC'D + AB' + A'C + A'C'D]'$

$= [D' + AC' + AB' + A' [C + C'D]]'$

$= [D' + AC' + AB' + A' [C + D]]'$

$= [D' + AC' + AB' + A'C + A'D]'$

$(\because \quad D' + A'D = D' + A')$

$= [D' + A' + AC' + AB' + A'C]'$

$(\because A' + A'C = A')$

$(\because A' + AC' + AB' = A'+A(C'+B') = A' + C' + B')$

$= [D' + A' + C' + B']'$

$= ABCD$

Hence, only 1 minterm is required.

15. (d)

Let,

A =		a_2	a_1	a_0
B =			b_1	b_0
A × B =		a_2b_0	a_1b_0	a_0b_0
	b_1a_2	b_1a_1	b_1a_0	↓
	b_1a_2	$(a_2b_0 + a_1b_1)$	$(a_1b_0 + b_1a_0)$	a_0b_0
	C_3	C_2	C_1	C_0

Number of AND gates required X = 6

Number of one bit full adders required Y = 3

$X + Y = 6 + 3 = 9$

16. (d)

Output of ExOR Gate = $b_i \oplus b_{i+1}$

Initially $Q = 0$ assume

So, After 1 clock, $Z = b_7 \oplus b_0$

After 2 clock, $Z = b_7 \oplus b_6$

After 3 clock, $Z = b_6 \oplus b_5$

After 4 clock, $Z = b_5 \oplus b_4$

After 5 clock, $Z = b_4 \oplus b_3$

After 6 clock, $Z = b_3 \oplus b_2$

After 7 clock, $Z = b_2 \oplus b_1$

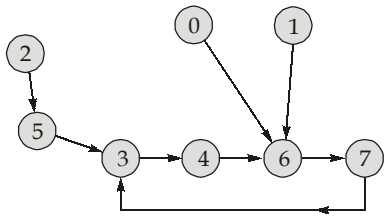
After 8 clock, $Z = b_1 \oplus b_0$

Which is same as Binary to gray code converter.

17. (d)

Test for Lockout

Present State			Present Input						Nest State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1



Hence, the counter does not enter into lockout state.

18. (a)

After 1st clock tick:

$$x_0^+ = x_0$$
$$x_1^+ = x_0 \oplus x_1$$
$$x_2^+ = (x_0 + x_1) \oplus x_2$$
$$x_3^+ = (x_0 + x_1 + x_2) \oplus x_3$$

After 2nd clock tick:

$$(x_0^+)^+ = x_0^+ = x_0$$
$$(x_1^+)^+ = x_0^+ \oplus x_1^+ = x_0 \oplus x_0 \oplus x_1 = 0 \oplus x_1 = x_1$$
$$(x_2^+)^+ = (x_0^+ + x_1^+) \oplus x_2^+ = \underbrace{(x_0 + (x_0 \oplus x_1))}_{A} \oplus \underbrace{(x_0 + x_1)}_{B} \oplus x_2$$

x_1	x_0	A $(x_0 + (x_0 \oplus x_1))$	B $(x_0 \oplus x_1)$	A ⊕ B
0	0	0	0	0
0	1	1	1	0
1	0	1	1	0
1	1	1	1	0

$= 0 \oplus x_2 = x_2$ [By using above truth table]

$$(x_3^+)^+ = (x_0^+ + x_1^+ + x_2^+) \oplus x_3^+$$
$= x_3$ only

So, after 2 clock tick Register R contain X only.

19. (b)

We know that, for Mod-N counter $f_o = \frac{f_i}{N}$

f_o = Output frequency = 8 kHz
f_i = Input frequency = 256 kHz

$$\text{Mod N} = \frac{f_i}{f_0}$$

$$= \frac{256\text{ kHz}}{8\text{ kHz}} = 32$$

20. (a)

Exponent = 1000 0101 = 133
Biased exponent = Actual exponent + Bias
Actual exponent = Biased exponent – Bias
= 133 – 127 = 6
Mantissa = 11010000000000000000000
Number = 1.1101×2^6
= –1110100
= $(-116)_{10}$

21. (d)

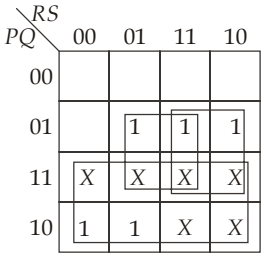
- S_1 is incorrect, as mentioned in question would required five 4X1 MUX instead of three.
- S_2 is incorrect, as it is not always the case. For example, the function $f(x, y, z) = \Sigma_m(2, 4, 5, 6)$ can have different PI when group differently in K-map.

22. (a)

Truth table for BCD to excess-3 code output:

Decimal Value	Input				Output				Decimal Value
	P	Q	R	S	P	Q	R	S	
0	0	0	0	0	0	0	1	1	3
1	0	0	0	1	0	1	0	0	4
2	0	0	1	0	0	1	0	1	5
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
5	0	1	0	1	1	0	0	0	8
6	0	1	1	0	1	0	0	1	9
7	0	1	1	1	1	0	1	0	10
8	1	0	0	0	1	0	1	1	11
9	1	0	0	1	1	1	0	0	12

K-map for P: $f(P, Q, R, S) = \Sigma m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$



$= P + QS + QR$
$= P + Q(S + R)$

23. (b)

$$Y = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

$$I_0 = I_3 = S_1 \text{ and } I_1 = I_2 = S_0$$

So, $$Y = \bar{S}_1\bar{S}_0S_1 + \bar{S}_1S_0S_0 + S_1\bar{S}_0S_0 + S_1S_0S_1$$

$$= \bar{S}_1S_0 + S_1S_0 = S_0$$

So, whenever $S_0 = B$, output $(Y) = B$
So, option (b) is correct.

24. (b)

We consider the last full adder far worst case delay.
Time after which output carry bit becomes available from the last full adder.
= total number of full address × carry propagation delay of full adder.
= 16 × 12 ns = 192 ns
Time after which output sum bit becomes available from the last full adder.
= time taken for its carry in to become available + sum propagation delay of full adder.
= {total number of full address before last full adder × carry propagation delay of full adder} + sum propagation delay of full adder.
= {15 × 12 ns} + 15 ns = 195 ns

25. (d)

$$A \oplus B = 10101101 \oplus 01101100 = 11000001$$

Now convert above binary code to gray code.
Gray of (11000001) is $(10100001)_2$

$$(10100001)_2 = (161)_{10}$$

26. (b)

CLK	Q_0	Q_1	Q_2	J_0 K_0	J_1 K_1	J_2 K_2	$\bar{Q}_1$ $\bar{Q}_2$ (2 input gate)
0	0	0	0	1 1	1 1	1 1	1 1
1	1	0	0	1 1	1 1	1 1	1 1
2	0	1	0	1 1	1 1	1 1	0 1
3	1	1	0	1 1	1 1	1 1	0 1
4	0	0	1	1 1	1 1	1 1	1 0
5	1	0	1	1 1	1 1	1 1	1 0
6	0	1	1	1 1	1 1	1 1	0 0

Now if we will use OR gate then the flip flop will be CLR and we will get mod-6 counter from (0 to 5).

27. (d)

All the above statements are correct.

28. (a)

Clock	$S.I = Y$	Q_3	Q_2	Q_1	Q_0
		0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	1	1	1	1	1
5	0	0	1	1	1 ← Required Content

Total 5 clock cycles are required.

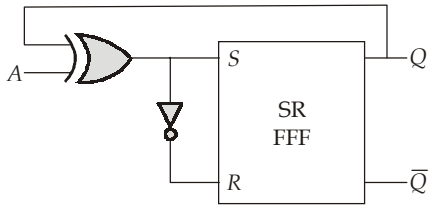
29. (c)

$$\text{Output of MUX} = \bar{A}Q + A\bar{Q}$$

Output of decoder, $S = \bar{A}Q + A\bar{Q}$

$$R = \overline{\bar{A}Q + A\bar{Q}}$$

So,



In SRFF

$$Q_{n+1} = S + \bar{R}Q_n$$
$$= (A \oplus Q_n) + \left(\overline{A \oplus Q_n}\right)Q_n$$
$$= A \oplus Q_n$$

So, Q_{n+1} is excitation equation of T-flip flop. Thus, the circuit will function as T-flip flop.

30. (a)

Johnson counter with n-flip flops has $2n$ state.

Here, $n = 4$

So total state is = 8

$= n \times 2 + 0.1$ ms

$= 8 \times 2 + 0.1 = 16.1$ ms

■■■■