CLASS TEST

Sl.: 01SK_DEFGHIJKL_151024

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Date of Test : 15/10/2024

ANSWER KEY

1.	(d)	7.	(b)	13.	(b)	19.	(b)	25.	(b)
2.	(b)	8.	(a)	14.	(c)	20.	(b)	26.	(d)
3.	(b)	9.	(c)	15.	(d)	21.	(d)	27.	(b)
4.	(c)	10.	(d)	16.	(c)	22.	(d)	28.	(b)
5.	(a)	11.	(b)	17.	(a)	23.	(d)	29.	(c)
6.	(c)	12.	(c)	18.	(b)	24.	(d)	30.	(a)

DETAILED EXPLANATIONS

1. (d)

- Since, vertical microprogram encode the control signals hence a signal decoder is needed which decrease the operational speed of vertical micro-programming in comparison with horizontal micro-programming.
- Since, the control signal bits under horizontal microprogram control unit are not encoded. Hence no signal decoder is needed.

2. (b)

$$ET_{\text{non-pipe}} = \text{Average CPI} \times \text{Cycle time (non-pipe)}$$
$$= 5 \times 0.25\ \mu\text{sec} = 1.25\ \mu\text{sec}$$
$$ET_{\text{pipe}} = \text{Average CPI}_{\text{pipe}} \times \text{Cycle time (pipe)}$$
$$= 1 \times 0.33\ \mu\text{sec} = 0.33\ \mu\text{sec}$$
$$\text{Speed-up} = \frac{ET_{\text{non-pipe}}}{ET_{\text{pipe}}} = \frac{1.25}{0.33} = 3.78 \approx 3.7$$

3. (b)

Format of single precision floating point is

32 bits

S	Exponant	Mantissa
1 bit	8 bits	23 bits

0	1 0 0 0 0 1 1 1	101000000000...00

$$\text{Value} = 1.M \times 2^{E-127}$$
$$= 1.1010 \times 2^{135 - 127}$$
$$= (1.1010)_2 \times 2^8$$
$$= 1.625 \times 2^8$$
$$= (416)_{10}$$

Octal representation

8	416	
8	52	0
	6	4

Octal representation is (640).

4. (c)

238715	I_1
238716	I_1
238717	I_1
238718	I_1
238719	I_1
238720	
238721	

(238715–238719) Fetch I_1 IR: PC = 238720

$$\text{Effective address} = \text{PC} + \text{Relative value}$$
$$= 238720 + (-32) = 238688$$

5. **(a)**

Given:

Group-1 and 2 are using horizontal micro-programming,

Hence, total bits are:

$$3 + 9 = 12$$

Group-3, 4 and 5 are using vertical micro-programming,

Hence, total bits are:

$$\lceil \log_2 6 \rceil + \lceil \log_2 13 \rceil + \lceil \log_2 10 \rceil = 3 + 4 + 4 = 11$$

Total bits for control word $= 12 + 11 = 23$ bits

6. **(c)**

- More than one word are put in one cache block to explicit in the spatial locality of reference.
- By the help of virtual memory, programs can exceed from the size of primary memory, hence increases the degree of multi programming.
- Increasing RAM will result in fewer page faults.

Hence only S_2 is the correct statement.

7. **(b)**

For 1 second it take 10^9 byte

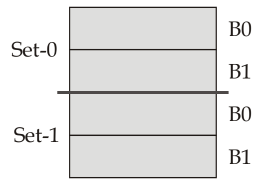
So for 64 kbyte it takes $= \dfrac{64k}{10^9} = 64\ \mu\text{sec}$

Main memory latency = 64 μsec

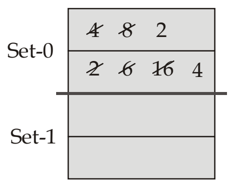
Total time required to fetch = 64 μsec + 64 μsec = 128 μsec

8. **(a)**

Cache will be divided as,

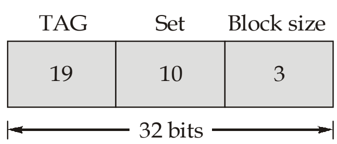


Since block addresses 4 and 2 are already there,



Total number of misses= 5

9. **(c)**



$$\text{Number of lines} = \frac{32 \times 2^{10}\,\text{B}}{2^3\,\text{B}} = 2^{12}$$

$$\text{Number of set} = \frac{2^{12}}{4\,\text{Way}} = 2^{10}$$

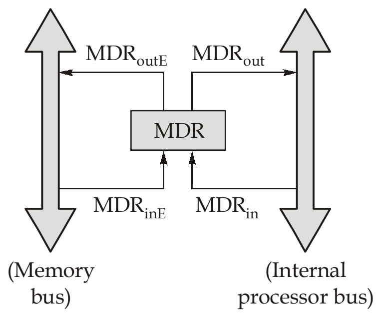
TAG bit	Set	Block
1111 1010 1111 1110 111	01011 11100	001

Set = 0101111100 = 380

10. **(d)**

Considering each statement:

S_1 : 4-control signals are needed for each data register.



MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

S_2 : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

11. **(b)**

Average cycles/instruction = {(0.2 × 0) + (0.2 × 0) + (0.4 × 16) + (0.2 × 12)}
= {6.4 + 2.4} = 8.8 cycles

So, average time = 8.8 nsec

1 operand requires 8.8 nsec

Number of operands fetched in 1 sec

$$\text{Number of operands} = \frac{1\text{ sec}}{8.8\text{ nsec}} = 0.113636 \times 10^9 \text{ operand/sec}$$

Operand fetch rate = 113.636 million words/sec

12. **(c)**

$$\text{Speedup (S)} = \frac{1}{(1-\text{Cache \% used}) + \left[\dfrac{\text{Cache \% used}}{\text{Speedup using cache}}\right]}$$

$$= \frac{1}{(1-F)+\left(\dfrac{F}{S}\right)} = \frac{1}{(1-0.9)+\left(\dfrac{0.9}{30}\right)} = \frac{1}{(0.1)+\left(\dfrac{0.9}{30}\right)}$$

$$= \frac{30}{3.9} = 7.69$$

13. (b)

	Instruction	Instruction size	Location
I_1	Load r_0, 300	2 word	2000-2003
I_2	MOV r_1, 5000	2 word	2004-2007
I_3	MOV r_2, (r_1)	1 word	2008-2009
I_4	Add r_0, r_2	1 word	2010-2011
I_5	MOV, 6000, r_0	2 word	2012-2015
I_6	HALT	1 word	2016-2017

$\therefore$ Since 1 word is of 2 bytes.

If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address 2016 is saved in the stack.

14. (c)

The minimum number of clock cycles can be obtained by writing its assembly code. The process in obtaining the outputs Z and R from input line X or Y via the same manner, such that the codes are not much different except there is a line code to execute store command when using input line X. The code is as follows:

	Instruction	**Meaning**	
I_1 :	Load ACC, R	ACC $\leftarrow$ (R)	{R = A_i}
I_2 :	Inc, R	R $\leftarrow$ (R) + 1	
I_3 :	Mul ACC, R	ACC $\leftarrow$ (ACC) × (R)	
I_4 :	Store R, ACC	R $\leftarrow$ (ACC)	

Constructing the table:

	1	2	3	4	5	6	7
I_1	F	D	E	W			
I_2		F	D	E	W		
I_3			F	D	E	W	
I_4				F	D	E	W

So, the minimum clock cycles required to complete one process is 7 clock cycles.

15. (d)

$$\text{Main memory size} = 32768 \text{ blocks}$$
$$1 \text{ block} = 512 \text{ words}$$
$$= 32768 \times 512 \text{ words} = 2^{15} \times 2^9 = 2^{24} \text{ words}$$

Main memory takes 24 bits.

$$\text{Block size} = 512 \text{ words} = 2^9 \text{ words}$$

Number of bits for block size = 9 bits.

Number of blocks in set associative = 128

Number of blocks in one set = 4

$$\text{Number of sets in cache} = \frac{128}{4} = 32 = 2^5$$

Number of bits in set offset = 5 bits

24

TAG	SET OFFSET	WORD OFFSET
10	5	9

Number of TAG bits = 24 – (9 + 5) = 10 bits

16. (c)

$$T_{avg} = h_1 t_1 + (1 - h_1)h_2 (t_2 + t_1) + (1 - h_1)(1 - h_2)(t_3 + t_2 + t_1)$$
$$= 0.65 \times 0.02 + 0.35 \times 0.45 \times 0.22 + 0.35 \times 0.55 \times 2.22$$
$$= 0.013 + 0.03465 + 0.42735$$
$$= 0.475 = 475\ \mu sec$$

17. (a)

DMA transfer character at rate of 19200 bpsec

8 bit = 1 character

So, 192000 bit = 2400 character

So, 1 sec = 2400 character

$$1 \text{ character (X)} = \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec}$$
$$= 416.6\ \mu sec$$

Processor fetch rate is 2 MIPS

1 MIPS = 1 sec

$$1 \text{ Instruction (Y)} = \frac{1}{2 \times 10^6} = 0.5\ \mu sec$$

$$\%\text{ slow down using DMA} = \left(\frac{Y}{X+Y}\right) \times 100$$
$$= \left(\frac{0.5}{416.6 + 0.5}\right) \times 100 = 0.11\%$$

18. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

19. (b)

Programmed I/O: Processor issues an IO command, on behalf of a processor, to an IO module; that process then busy-waits for the operation to be completed before proceeding.

Interrupt driven I/O: The processor issues an IO command on behalf of a process, continues to execute subsequent instruction, and is interrupted by the IO module when the latter has completed its work.

Direct memory access: A DMA module controls the exchange of data between main memory and IO module.

20. (b)

$$\text{Number of lines} = \frac{16\text{ KB}}{32\text{ B}} = \frac{2^{14}}{2^5} = 2^9$$

$$\text{Number of sets} = \frac{2^9}{2^2} = 2^7$$

$$\text{Physical address size} = 256\text{ MB} = 28\text{ bits}$$

28 bit

TAG	SO	WO
16 bit	7 bit	$\log_2 32 = 5$ bit

Total set will be from 0 to 127 (using 7 bits).
In option (b)

$(FB3D64C)_{16}$ = F B 3 D 0 1 1 0 0 1 0 0 C

- F B 3 D → 16 bit TAG
- 0 1 1 0 0 1 0 → 7 bit set → It's decimal value is 50
- 0 C → 5 bit WO

Hence option (b) is correct.

21. (d)

	1	2	3	4	5	6	7	8	9	10	11
I_1	IF	ID	EX	MM	WB						
I_2		IF	ID	ID	EX	MM	WB				
I_3			IF	IF	ID	EX	MM	WB			
I_4					IF	ID	EX	MM	WB		
I_5						IF	ID	ID	EX	MM	WB

Total 11 cycles are required.

22. (d)

IF	ID	OF	PD and WB
I_1 : 1 memory reference	2 memory reference	1 memory reference	–
I_2 : 1 memory reference	3 memory reference	2 memory reference	–
I_3 : 1 memory reference	1 memory reference	–	1 ALU operation
I_4 : 1 memory reference	3 memory reference	2 memory reference	–
I_5 : 1 memory reference	–	–	1 ALU operation

Total Execution Time = (Number of memory reference × 3 cycles + Number of ALU operation × 1 cycles) × cycle time

$$= (19 \times 3 + 2 \times 1) \times \frac{1}{5\text{ GHz}} = \frac{59}{5}\text{ ns} = 11.8\text{ ns}$$

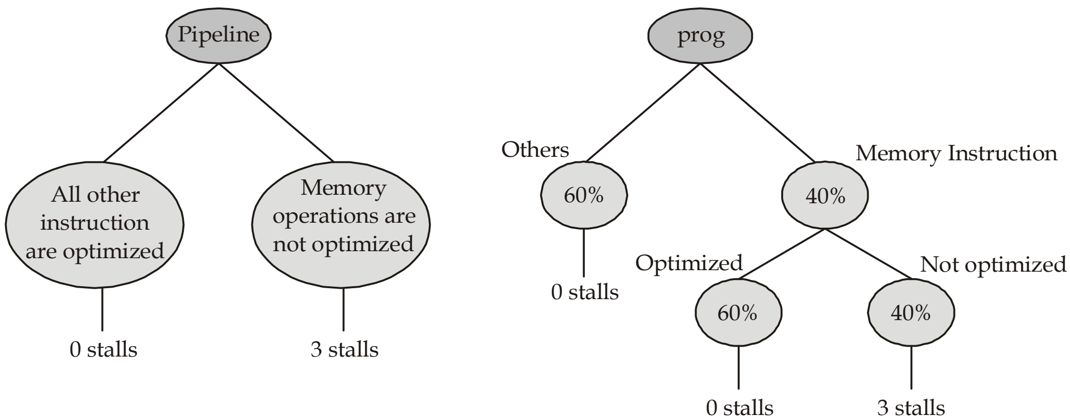
23. (d)

- Hardwired control unit design is not suitable in design and testing places because small modification change the working of whole system. So, we have to design again.
- Horizontal control unit design is implemented using sum of product expression on a flip-flops.
- Vertical micro programmed control unit allows low degree of the parallelism, whereas horizontal micro programmed control unit allows high degree of the parallelism.
- In the control unit design control signals are represented in a encoding format/decoding format/SOP format.

24. (d)

(i) is true, it is logically done.
(ii) is false, structural dependency resolved using re-naming.
(iii) Delayed branch re-arranges code to reduce control dependency.

25. (b)



Number of stalls/Instruction = $(0.4 \times 0.4 \times 3) = 0.48$

Average instruction ET = (1 + # stalls / Instruction) × Cycle time

= $(1 + 0.48) \times 8$ ns = 11.84 ns

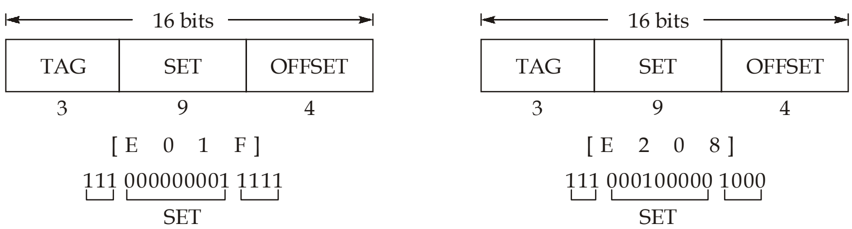
26. (d)

Block size = 16 byte = 2^4 byte = 4 bits

Blocks in main memory = 2^{10}

So number of sets = $\frac{2^{10}}{2^1} = 2^9 \Rightarrow 9$ bits

Number of bits in physical address = 2^{16} byte $\Rightarrow$ 16 bits



SET value_1 = 000000001 = Decimal value = $(1)_{10}$

SET value_2 = 000100000 = Decimal value = $(32)_{10}$

Difference = $\text{SET}_2 - \text{SET}_1$

= $32 - 1 = (31)_{10}$

27. (b)

Word addressable storage

3001 – 3002	$\rightarrow$	I_1
3003	$\rightarrow$	I_2
3004	$\rightarrow$	I_3
3005	$\rightarrow$	I_4
3006	$\rightarrow$	I_5
3007	$\rightarrow$	I_6
3008 – 3009	$\rightarrow$	I_7
3010	$\rightarrow$	I_8

Valid program counter value after program is 3010.

28. (b)

$$P_1 \text{ CPU time } = \frac{[1 \times 0.1 + 2 \times 0.1 + 3 \times 0.5 + 4 \times 0.3]}{1.5 \times 10^9}$$

$$= 2 \times 10^{-9} \text{ sec} = 2 \text{ nsec}$$

$$P_2 \text{ CPU time } = \frac{[2 \times 0.1 + 2 \times 0.1 + 2 \times 0.5 + 2 \times 0.3]}{2.5 \times 10^9}$$

$$= 0.8 \times 10^{-9} \text{ sec} = 0.8 \text{ nsec}$$

$\therefore$ P_2 is faster than P_1 processor.

29. (c)

The decimal number is = (– 48.625)

Binary number representation of (– 48.625)

Normalization form = 1.10000101×2^5

Mantissa field is = 10000101000000000000000

Exponent field is = $5 + 127 = 132 = (10000100)_2$

Value in given format is

Sign(s)	Exponent (E)	Mantissa (M)
1	100 00100	100 00101000000000000000000

C 2 4 2 8 0 0 0

So the hexadecimal representation is $(C2428000)_{16}$.

30. (a)

$$X = (A + B \times C)/(D - E \times F)$$

1-Address Machine:

1. LOAD E
2. MUL F
3. STORE T
4. LOAD D
5. SUB T
6. STORE F
7. LOAD B
8. MUL C
9. ADD A
10. DIV T
11. STORE X

So, total 11 instruction in 1-address machine.

2-Address Machine:

1. MOV R_0, E
2. MUL R_0, F
3. MOV R_1, D
4. SUB R_1, R_0
5. MOV R_0, B
6. MUL R_0, C
7. ADD R_0, A
8. DIV R_0, R_1
9. MOV X, R_0

Total 9 instructions in 1-address machine.

So, 2 extra instruction is required in 1-address machine.

■■■■