POSTAL Book Package 2023

ESE

Electronics Engineering

Conventional Practice Sets

Computer Organization and Architecture

Contents

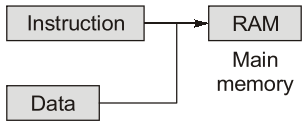
MADE EASY Publications

1 CHAPTER
Computer Organization

Q.1 Describe computer block diagram and list its internal components.

Solution:

Computer is a computational machine, used to process data under the control of a program. Computer system is implemented using Von Neumann architecture which says that instruction and data both are present in main memory.



Computer system contains 3-fundamental components:

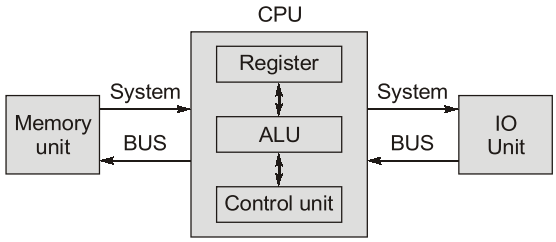
(i) **Central Processing Unit (CPU) :** . It contains 3 internal components
→ Registers → ALU → Control unit.

(ii) **Memory:** It is the storage component of computer. Memory chip is organised into cells called as addressable unit.

Ex: 64 KB RAM = 64 K × B → Cell Size
↓
Cells in chip

(iii) **IO:** It is external communication unit. It is of two kind as

(a) Input devices ($\overline{IORD}$) (b) Output devices ($\overline{IOWR}$)



Q.2 Explain different instruction format possible in computer design.

Solution:

CPU organisation is classified into 3-type:

(i) **Stack CPU :** In this organisation ALU operations are performed only on a stack data means both of the operands are always present in stack. After processing result is also present in stack.

(ii) **Accumulator CPU :** In this organisation ALU's 1st operand is always required in the accumulator and 2nd operand is present either is register or memory.
After processing result is always present in accumulator.

(iii) Register CPU :

(a) Register to memory reference CPU: In this organisation ALU 1st operand is always required in register and 2nd operand is present either in register or in memory. After processing result is placed in source-1 register.

(b) Register to register reference CPU: In this organisation, ALU operations are performed only on register data, means both of the operands are always required in register. After processing result in placed in 3rd register.

Q.3 List five distinct features each of the RISC based and the CISC based design of processors.

Solution:

RISC (Reduced Instruction Set Computer)	CISC (Complex Instruction Set Computer)
It requires multiple clock per instruction.	It requires one clock cycle per instruction.
More number of instruction	Less number of instruction.
More addressing modes	Few addressing mode.
It is hardwired.	It is micro programmed.
It is slower.	It is faster.

Q.4 Distinguish between

(i) High level language and low level language
(ii) Macro-Programming and Micro-Programming
(iii) Machine cycle and instruction cycle
(iv) Hardware interrupt and software interrupt
(v) Memory mapped I/O and I/O mapped I/O

Solution:

(i) Machine specific languages are known as low level language **e.g.** machine language and assembly languages are low level language.

While machine independent languages are high level language **e.g.** C, C++, JAVA, PASCAL.

(ii) Image's built in programming languages can be used to automate complex or repetitive task in case of microprogramming. Microcode is a layer of hardware level instruction and writing microcode is called as microprogramming. Macro instruction is a statement typically for an assembler that invokes a macro definition to generate a sequence of instructions. While microinstruction is hardware level instruction used for implementation of machine code.

(iii) Machine cycle is defined as cycle for accessing memory one time.

While instruction cycle is defined as cycle (total T states) required for execution of an instruction. An instruction cycle contains several machine cycles. **e.g.** MVI M, 20 H contains 3 machine cycle → 1 op-code fetch + 1 read + 1 write.

(iv) A hardware interrupt causes the processor to save its state of execution and begin execution of an interrupt handler.

Software interrupts are usually implemented as instructions in the instruction set, which causes a context switch to an interrupt handler similar to hardware interrupt.

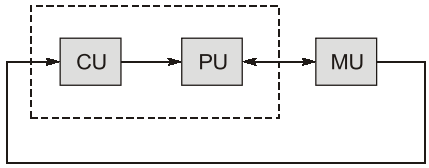
Trigger for hardware interrupt is an electrical signal while for software it is execution of machine language instruction.

(v) In memory mapped I/O address is of 16 bit while in I/O mapped i/o address is of 8 bit. All memory related instructions are used in memory mapped I/O while IN and OUT instructions are only used in case of I/O mapped. Arithmetical or logical operations can be directly performed in case of memory mapped I/O with I/O data while it is not possible in case of I/O mapped.
In case of memory mapped i/o memory is shared between I/Os and system memory. While I/O mapped is independent of memory map.
In case of memory mapped more hardware needed compare to that of i/o mapped I/O.

Q.5 Explain Flynn's classification of computer design?

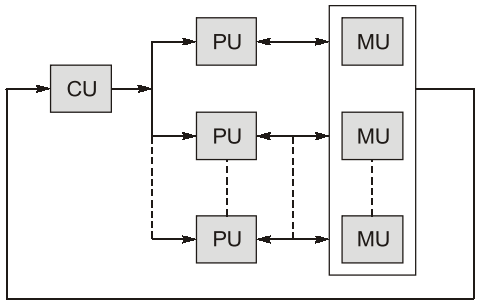
Solution:

(a) **Single Instruction Single Data (SISD) :** No concurrency in this computer.



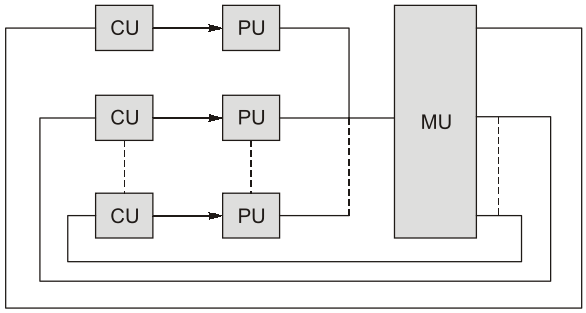
Ex : 8085

(b) **Single Instruction Multiple Data (SIMD) :** Data level concurrency is present



Ex : Staran processor.

(c) **Multiple Instruction Single Data (MISD) :** This architecture contains multiprocessor but only one processor is used at a time.



(d) **Multiple Instruction Multiple data (MIMD) :** This architecture contains instruction level concurrency.