POSTAL Book Package 2023

GATE

Electronics Engineering

Objective Practice Sets

Computer Organization

Contents

MADE EASY Publications

1 CHAPTER
Machine Instructions and Addressing Modes

MCQ and NAT Questions

Q.1 The computer performs all mathematical and logical operations inside its

(a) Memory unit (b) Central processing unit
(c) Output unit (d) Visual display unit

Q.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Pointer
B. Position Independent code
C. Constant operand

List-II

1. Indirect AM
2. Immediate AM
3. Relative AM

Code:

	A	B	C
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Q.3 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.4 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?

(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.5 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.

(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.6 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.7 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:

X. Indirect addressing
Y. Indexed addressing
Z. Base register addressing

Column 2:

1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.64 Consider the following statements. Which of the following is correct for the computers that uses memory mapped I/O?

(a) The computer provides special instruction for manipulating I/O port.

(b) I/O ports are placed at address on bus and as accessed just like other memory location.

(c) To perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.

(d) Ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

Q.65 Consider a hypothetical system which has 32 bit instruction size and 8 bit address. If there are 180 2-address instructions and 400 one 1-address instruction then which of the following are correct?

(a) Total opcodes possible is 2^{12}.

(b) Number of 1-address instruction
$= (2^{16} - 180) \times 2^8$

(c) Number of zero-address instruction
$= ((2^{16} - 180) \times 2^8 - 400) \times 2^8$

(d) Number of zero-address instruction
$= (2^{16} - 180 \times 2^8 - 400) \times 2^8$

Q.66 Which of the following statement are correct?

(a) Address decoder is an essential part of I/O interface.

(b) Compared to RISC processor CISC processor contains large instruction set and less number of registers.

(c) Separate I/O address space does not necessarily mean that I/O address lines are physically separated.

(d) None of these

■■■■

Answers Machine Instructions and Addressing Modes

1.	(b)	**2.**	(c)	**3.**	(a)	**4.**	(c)	**5.**	(a)	**6.**	(a)	**7.**	(a)
8.	(c)	**9.**	(a)	**10.**	(c)	**11.**	(c)	**12.**	(c)	**13.**	(d)	**14.**	(369)
15.	(16383)	**16.**	(b)	**17.**	(b)	**18.**	(d)	**19.**	(c)	**20.**	(3009)	**21.**	(d)
22.	(d)	**23.**	(c)	**24.**	(c)	**25.**	(d)	**26.**	(c)	**27.**	(b)	**28.**	(c)
29.	(d)	**30.**	(b)	**31.**	(c)	**32.**	(b)	**33.**	(c)	**34.**	(c)	**35.**	(c)
36.	(369)	**37.**	(a)	**38.**	(c)	**39.**	(b)	**40.**	(a)	**41.**	(–128)	**42.**	(a)
43.	(a)	**44.**	(d)	**45.**	(a)	**46.**	(d)	**47.**	(16)	**48.**	(b)	**49.**	(c)
50.	(a)	**51.**	(92)	**52.**	(2032)	**53.**	(c)	**54.**	(a)	**55.**	(b)	**56.**	(c)
57.	(c)	**58.**	(2048)	**59.**	(d)	**60.**	(a)	**61.**	(a, b, d)	**62.**	(c)	**63.**	(b, c)
64.	(b)	**65.**	(b, c)	**66.**	(a, b, c)								

Explanations **Machine Instructions and Addressing Modes**

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

Memory size = 4 GB = 2^{32} B

Word size = 2 B

So, unique address = $\frac{2^{32}}{2^{1}} = 2^{31}$

Hence, atleast 31 bits are required.

5. (a)

Each instruction is stored in one word of memory.

Memory is word addressable and 1 word = 24 bits $\Rightarrow$ 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

6. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

8. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

9. (a)

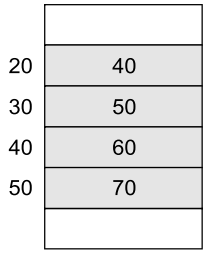
The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

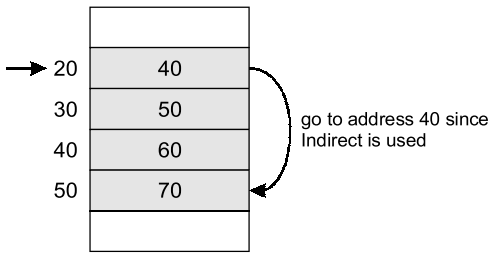
= 3012 H – 7 H = 300 BH

11. (c)

The given information can be understood as



Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

13. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.