

POSTAL Book Package

2023

Electrical Engineering

Conventional Practice Sets

Computer Fundamentals

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Q.1 Find the minimum product of sums of the following expression:

$$f = ABC + \bar{A}\bar{B}\bar{C}$$

Solution:

In order to find the minimum product of sums we must calculate what are the max terms.

We have SOP function as:

$$f = ABC + \bar{A}\bar{B}\bar{C}$$

⇒ Minimum terms are (0, 7)

Thus, maximum terms = (1, 2, 3, 4, 5, 6)

By using K-map

Hence, minimum product of sum will be $(\bar{A} + B)(A + \bar{C})(\bar{B} + C)$

BC \ A	00	01	11	10
0	0	0	0	1
1	1	1		1

Q.2 Show with the help of a block diagram represent Boolean function:

$$f = AB + BC + CA$$

can be realised using only 4 : 1 multiplexer.

Solution:

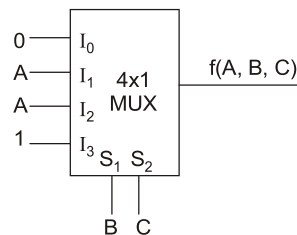
$$f = AB + BC + CA$$

A \ BC	00	01	11	10
0	0 ₀	0 ₁	1 ₃	0 ₂
1	0 ₄	1 ₅	1 ₇	1 ₆

Using MSB method:

	I ₀	I ₁	I ₂	I ₃
\bar{A}	0	1	2	③
A	4	⑤	⑥	⑦
	0	A	A	1

Implementing $f(A, B, C)$ using 4×1 MUX



Q3 A logic network has two data inputs A and B , and two control inputs C_0 and C_1 . It implements the function F according to the following table.

C_1	C_0	F
0	0	$\overline{A+B}$
0	1	$A+B$
1	0	$A \oplus B$
1	1	AB

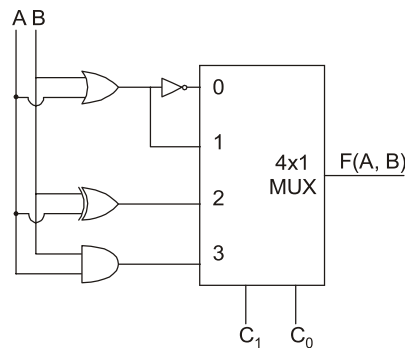
Implement the circuit using one 4 to 1 Multiplexer, one 2-input Exclusive OR gate, one 2-input AND gate, one 2-input OR gate and one Inverter.

Solution:

I_0 will get activated when both the select lines are zero thus I_0 will intake $\overline{A+B}$.

I_1 will get activated when C_1 is 0 and C_0 is 1 thus I_1 will intake $A+B$.

Similarly, I_2 will intake $A \oplus B$ and I_3 will intake AB .



Q4 Find the minimum sum of products form of the logic function.

$$f(A, B, C, D) = \sum m(0, 2, 8, 10, 15) + \sum d(3, 11, 12, 14)$$

Where m and d denote the min-terms and don't cares respectively.

Solution:

$$f(A, B, C, D) = \sum m(0, 2, 8, 10, 15) + \sum d(3, 11, 12, 14)$$

CD \ AB	00	01	11	10
00	1 ₀	1	x ₃	1 ₂
01		4	5	7
11	x ₁₂		1 ₁₅	x ₁₄
10	1 ₈		x ₁₁	1 ₁₀

The minimum SOP form of the logic function is given as: $f(A, B, C, D) = B'D' + AC$.

Q5 Express the function $f(x, y, z) = xy' + yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.

Solution:

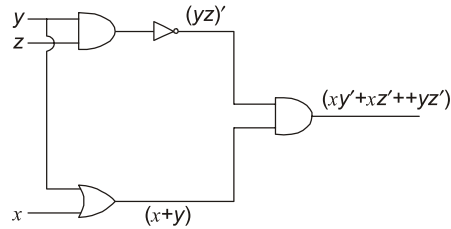
To use only single NOT gate, express it with only one complementation and one or more AND/OR operations.

$$f(x, y, z) = xy' + yz'$$

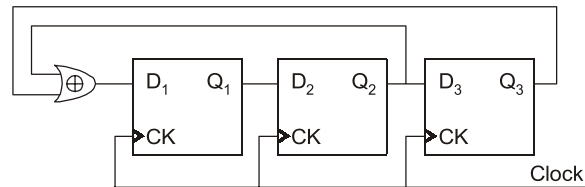
Add reduced term to f

$$\begin{aligned}
 f(x, y, z) &= xy' + yz' + xz' \\
 &= yz' + x(y' + z') \\
 &= y(y' + z') + x(y' + z') \\
 &= (x + y)(y' + z') = (x + y)(yz)'
 \end{aligned}$$

Thus the given function has been represented using one complement operation with complement on yz .
Logic circuit implementing the expression obtained is given as below:



Q6 Consider the synchronous sequential circuit in figure.



(a) Draw a state diagram which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

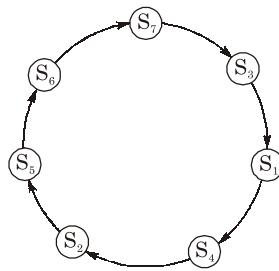
0	0	0	S_0
0	0	1	S_1
0	1	0	S_2
0	1	1	S_3
1	0	0	S_4
1	0	1	S_5
1	1	0	S_6
1	1	1	S_7

(b) Given that the initial state of the circuit is S_4 , identify the set of states which are not reachable.

Solution:

$D_1(Q_2 \oplus Q_3)$	$D_2(Q_1)$	$D_3(Q_2)$	Q_1	Q_2	Q_3	State
			1	1	1	(S_7)
0	1	1	0	1	1	(S_3)
0	0	1	0	0	1	(S_1)
1	0	0	1	0	0	(S_4)
0	1	0	0	1	0	(S_2)
1	0	1	1	0	1	(S_5)
1	1	0	1	1	0	(S_6)
1	1	1	1	1	1	(S_7)

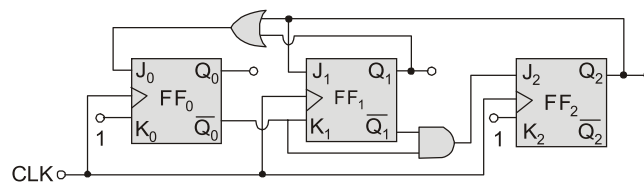
(a) The state diagram which is implemented by the circuit is as follows:



(b) If the initial state of the circuit is S_4 , then the state which is not reachable is S_0

$S_4 \rightarrow S_2 \rightarrow S_5 \rightarrow S_6 \rightarrow S_7 \rightarrow S_3 \rightarrow S_1$

Q.7 For the synchronous counter shown in figure write the truth table of Q_0 , Q_1 and Q_2 after each pulse starting from $Q_0 = Q_1 = Q_2 = 0$ and determine the counting sequence and also the modulus of the counter.



What is the modulus of the counter with initial state $Q_2 Q_1 Q_0 = 000$?

- (a) 3 (b) 4
(c) 5 (d) 6

Solution: (c)

J_2 ($\bar{Q}_0 \bar{Q}_1$)	K_2 (1)	J_1 (Q_2)	K_1 (\bar{Q}_0)	J_0 ($Q_1 + Q_2$)	K_0 (1)	Q_2	Q_1	Q_0
Initially						0	0	0
1	1	0	1	0	1	1	0	0
1	1	1	1	1	1	0	1	1
0	1	0	0	1	1	0	1	0
0	1	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0	0

There are 5 different states in the synchronous counter.

Therefore, the modulus of the counter is 5.

Q.8 Analyse the circuit in figure and complete the following table:

a	b	Q_n
0	0	
0	1	
1	0	
1	1	

