POSTAL Book Package 2023

Electrical Engineering

Objective Practice Sets

Computer Fundamentals

Contents

MADE EASY Publications

1 CHAPTER
Memory Organization and IO Organization

Q.1 More than one word are put in one cache block to
(a) Exploit the temporal locality of reference in a program.
(b) Exploit the spatial locality of reference in a program.
(c) Reduce the miss penalty.
(d) None of the above

Q.2 The access time of a word in a 4 MB main memory is 100 ns. The access time of a word in a 32 kB data cache memory is 10 ns. The average data cache hit ratio is 0.95. The effective memory access time is
(a) 9.5 ns (b) 15 ns
(c) 20 ns (d) 50 ns

Q.3 A memory system of size 128 K bits is required to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is
(a) 64 (b) 4
(c) 8 (d) 16

Q.4 A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least
(a) 32 bits (b) 31 bits
(c) 35 bits (d) 34 bits

Q.5 For the daisy chain scheme of connecting I/O devices, which of the following statements is true?
(a) It gives non-uniform priority to various devices.
(b) It gives uniform priority to all devices.
(c) It is only useful for connecting slow devices to a processor.
(d) It requires a separate interrupt pin on the processor for each device.

Q.6 The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set
(a) (k mod m) of the cache
(b) (k mod c) of the cache
(c) (k mod 2 c) of the cache
(d) (k mod 2 cm) of the cache

Q.7 When an interrupt occurs, an operating system
(a) ignores the interrupt
(b) always changes state of interrupted process after processing the interrupt
(c) always resumes execution of interrupted process after processing the interrupt
(d) may change state of interrupted process to 'blocked' and schedule another process

Q.8 A system uses FIFO policy for page replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?
(a) 196 (b) 192
(c) 197 (d) 195

Q.9 If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?
(a) Width of tag comparator
(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

Q.10 According to temporal locality, processes are likely to reference pages that
(a) have been referenced recently.
(b) are located at address near recently referenced pages in memory.
(c) have been preloaded in memory.
(d) None of these

Q.44 **Statement (I):** Most personal computers use static RAMs for their main memory.
Statement (II): Static RAMs are much faster than dynamic RAMs.

Q.45 **Statement (I):** Associative memory is fast memory.
Statement (II): Associative memory searches by content and not by accessing of address.

■■■■

Answers Memory Organization and IO Organization

1. (b)	2. (b)	3. (c)	4. (b)	5. (a)	6. (b)	7. (d)	8. (a)	9. (d)
10. (a)	11. (a)	12. (d)	13. (a)	14. (b)	15. (b)	16. (d)	17. (b)	18. (d)
19. (d)	20. (a)	21. (a)	22. (c)	23. (a)	24. (c)	25. (d)	26. (b)	27. (b)
28. (b)	29. (b)	30. (c)	31. (a)	32. (d)	33. (a)	34. (a)	35. (b)	36. (d)
37. (c)	38. (b)	39. (b)	40. (d)	41. (a)	42. (a)	43. (d)	44. (d)	45. (a)

Explanations Memory Organization and IO Organization

1. (b)

Spatial Locality : If a particular storage location is referenced at a particular time, then it is likely that nearby memory locations will be referenced in the near future. Thus keeping more than one block helps in using spatial locality concept.

2. (b)

Hit ratio, $H_c = 0.95$

Cache Memory Access Time

$T_c = 10$ ns

Main Memory Access Time

$T_m = 100$ ns

$EAT = H_c(T_c) + (1 - H_c)(T_c + T_m)$

$EAT = 0.95 \times 10 + 0.05 \times 110$

$EAT = 9.5 + 5.5$

$EAT = 15$ ns

3. (c)

Size of chip $= 2^{12} \times 4$ bits

Size of memory $= 128$ k bits

$$\text{Number of chips} = \frac{2^7 \times 2^{10}}{2^{12} \times 2^2} = 8$$

4. (b)

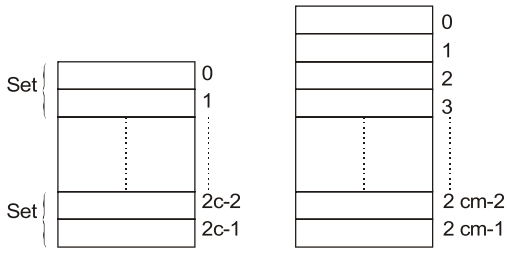
Total number of memory words (or) total number of memory addresses $= \frac{4 \times 2^{30}}{2} = 2 \times 2^{30} = 2^{31}$.

To represent 2^{31} addresses, at least 31 address lines are required.

5. (a)

The daisy-chaining method of establishing priority consists of a serial connection of all devices that request an interrupt. The device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the chain. The farther the device is from the first position, the lower is its priority. Therefore, daisy-chain gives non-uniform priority to various devices.

6. (b)



Number of set in set associative cache

$$= \frac{\text{number of blocks in cache}}{\text{number of blocks in one set}} = \frac{2c}{2} = c$$

Number of sets in cache = c

Therefore, the block k of the main memory maps to the set (k mod c) of the cache.

7. (d)

An interrupt is a signal from a device attached to a computer or from a program within the computer

that causes the main program that operates the computer to stop and figure out what to do next. After the interrupt signal is sensed, it may change state of interrupted process to 'blocked' and schedule another process.

8. (a)

FIFO policy for page replacement used.

Access 100 distinct pages by taking some example: 2 3 4 5 6 7 8 9

So by loading it get

5
4
3
2

= 4 page fault,

9
8
7
6

= 4 page fault

and now access these page in reverse so

9 8 7 6 — So no page fault for these

5 4 3 2 — page fault for these

9
8
7
6

5
4
3
2

4 page fault

So, total = 4 + 4 + 4 = 12 page fault

For 8 pages = 2 × 8 – 4 = 12

So, for n pages = 2n – 4

So, for 100 pages = 2 × (100) – 4 = 196

9. (d)

Assume,

Tag	Set	Word	
12	8	4	Here k = 4

⇓ when associativity doubled

Tag	Set	Word
13	7	4

- Since, tag bits have been changed thus width of a Tag comparator changes.
- Since, width of set bits changed thus width of a set index decoder.
- Width of multiplexor change since k changes.

10. (a)

Temporal locality says that recently executed instruction is likely to be executed very soon.

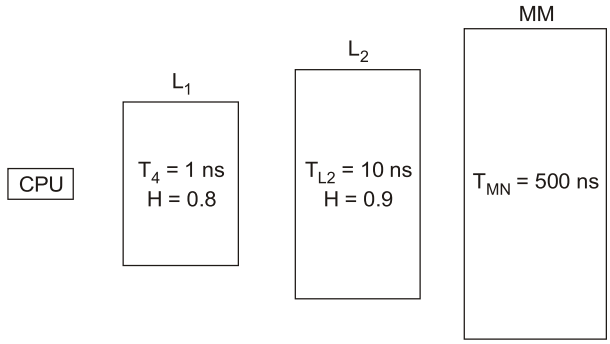
11. (a)

System which has lot of crashes, data should be written to the disk as soon as possible thus, write through cache is preferable.

12. (d)

Principle of locality states that many instruction in localized areas of the programs are executed repeatedly during short time period and the remainder of the program is accessed relatively less frequently. This is where use of cache comes into existence.

13. (a)



$$T_{avg} = 0.8 \times 1 + 0.2 \times 0.9 \times (1 + 10) + 0.2 \times 0.1 \times 511$$
$$= 0.8 + 1.98 + 10.22$$
$$= 13 \text{ ns}$$

14. (b)

$$T \geq 1.2\, T_c = 120$$
$$T = H.T_c + (1 - H)\,(T_m)$$
$$T = H.100 + (1 - H)\,(1200)$$
$$T = 100H + 1300 - 1200H$$
$$T = 1200 - 1200\, H \geq 120$$
$$1200\, H = 1200 - (120)$$
$$H = \frac{1200}{1200} - \frac{(120)}{1200}$$
$$H = 1 - 0.1 = 0.9$$

Hit Ratio = 90%

15. (b)

Average access time

= avg. seek time + avg. rotational latency + avg. transfer time

Here, for 1 round $= \frac{60\,\text{sec}}{n} = \frac{60{,}000}{n}$ msec

$\therefore$ Average rotational latency $= \frac{60{,}000}{2n}$

Also : 32 × 512 bytes = 1 track $= \frac{60{,}000}{n}$ msec