ESE

Electronics & Telecom. Engineering

Preliminary Examination

(Previous Years Solved Papers 1999)

Volume-I

Contents

MADE EASY PUBLICATIONS

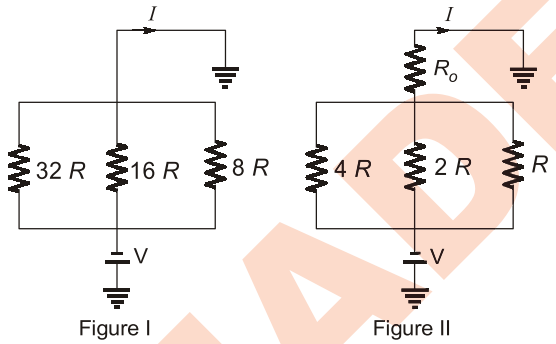
1 Network Theory

1. Basics of Network Analysis

1.1 An ideal constant voltage source is connected in series with an ideal constant current source. Considered together, the combination will be a
(a) constant voltage source
(b) constant current source
(c) constant voltage and a constant current source or a constant power source
(d) resistance

[ESE-1999]

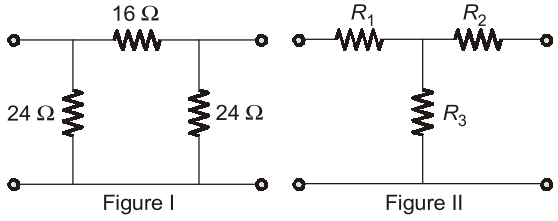
1.2 The circuit shown in Figure-I is replaced by that in Figure-II. If current 'I' remains the same, then R_0 then will be



(a) zero
(b) R
(c) $2R$
(d) $4R$

[ESE-1999]

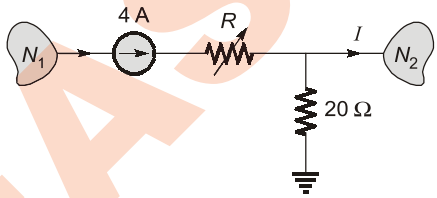
1.3 If the Π-network of Figure-I and T-network of Figure-II are equivalent, then the values of R_1, R_2 and R_3 will be respectively



(a) 9 Ω, 6 Ω and 6 Ω
(b) 6 Ω, 6 Ω and 9 Ω
(c) 9 Ω, 6 Ω and 9 Ω
(d) 6 Ω, 9 Ω and 6 Ω

[ESE-1999]

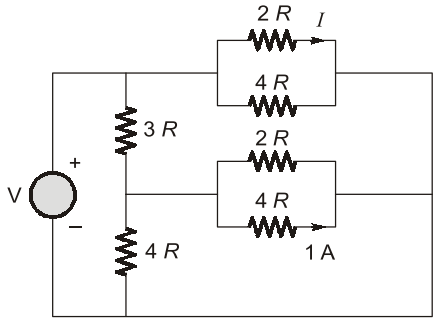
1.4 In the circuit shown in the figure, for $R = 20\ \Omega$ the current 'I' is 2 A. When R is 10 Ω, the current 'I' would be



(a) 1 A
(b) 2 A
(c) 2.5 A
(d) 3 A

[ESE-1999]

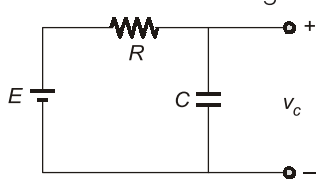
1.5 For the circuit shown in the figure, the current 'I' is



(a) indeterminable due to inadequate data
(b) zero
(c) 4 A
(d) 8 A

[ESE-1999]

1.6 Consider the following sets of values of E, R and C of the circuit shown in the figure



1. 2 V, 1 Ω and 1.25 F
2. 1.6 V, 0.8 Ω and 1 F
3. 1.6 V, 1 Ω and 0.8 F
4. 2 V, 1.25 Ω and 1 F

Which of these sets of E, R and C values will ensure that the state equation, $dv_c/dt = -1.25\ v_c + 2$ is valid?

(a) 1 and 4 (b) 1 and 2
(c) 3 and 4 (d) 2 and 3

[ESE-1999]

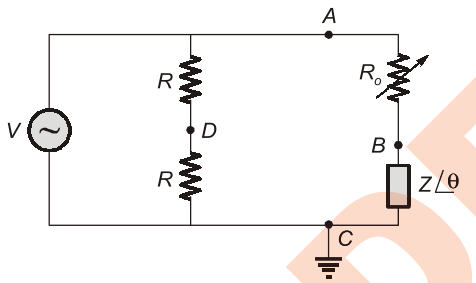
2. Steady State Sinusoidal Analysis & Resonance

2.1 A series resonant circuit has an inductive reactance of 1000 Ω, a capacitive reactance of 1000 Ω and a resistance of 0.1 Ω. If the resonant frequency is 10 MHz, then the bandwidth of the circuit will be

(a) 1 kHz (b) 10 kHz
(c) 1 MHz (d) 0.1 kHz

[ESE-1999]

2.2 In the circuit shown in the figure, if R_0 is adjusted such that $|V_{AB}| = |V_{BC}|$, then



(a) $\theta = 2\tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$

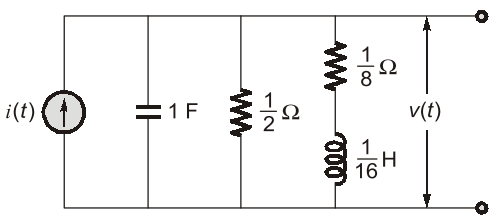
(b) $|V_{BC}| = |V_{DC}|$

(c) $|V_{AB}| = |V_{AD}|$

(d) $\theta = \tan^{-1}\left(\frac{|V_{BD}|}{|V|}\right)$

[ESE-1999]

2.3 In the circuit shown in the figure, $i(t)$ is a unit step current. The steady-state value of $v(t)$ is



(a) 2.5 V (b) 1 V
(c) 0.1 V (d) zero

[ESE-1999]

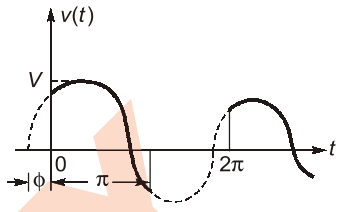
2.4 The average value of the periodic function $v(t)$ of the given figure is

(a) $\frac{V\cos\phi}{\pi}$

(b) $\frac{V\sin\phi}{\pi}$

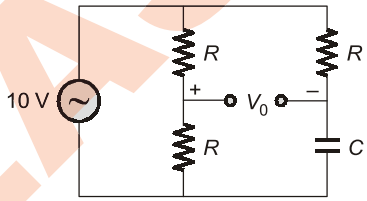
(c) $\frac{2V\cos\phi}{\pi}$

(d) $\frac{V}{\pi}$



[ESE-1999]

2.5 In the circuit shown in the figure, output $|V_0(j\omega)|$ is



(a) indeterminable as values of R and C are not given
(b) 2.5 V
(c) $5\sqrt{2}$ V
(d) 5 V

[ESE-1999]

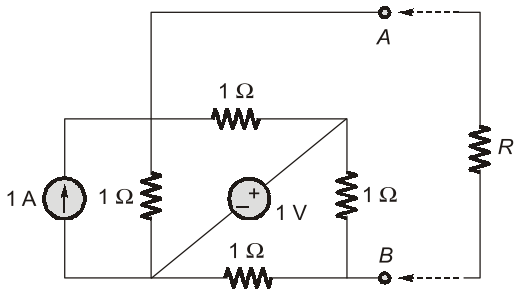
3. Network Theorems

3.1 **Assertion (A):** Tellegen's theorem is used in developing the sensitivity coefficient of a network from the concept of adjoint network.
Reason (R): Tellegen's theorem is applicable to any lumped network.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

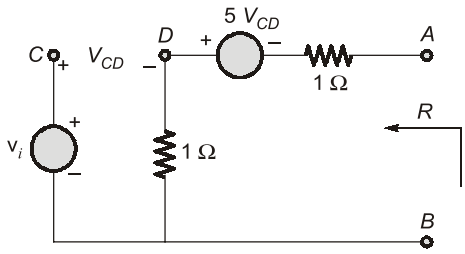
[ESE-1999]

3.2 If a resistance 'R' of 1 Ω is connected across the terminals AB as shown in the given figure, then the current flowing through R will be



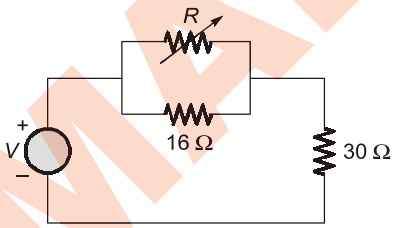
(a) 1 A (b) 0.5 A
(c) 0.25 A (d) 0.125 A **[ESE-1999]**

3.3 The resistance '*R*' looking into the terminals *AB* in the circuit shown in the figure will be



(a) 0.5 Ω (b) 2 Ω
(c) 3 Ω (d) 7 Ω **[ESE-1999]**

3.4 In the circuit shown in the figure, the power dissipated in 30 Ω resistor will be maximum if the value of *R* is

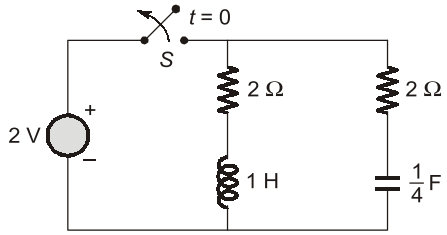


(a) 30 Ω (b) 16 Ω
(c) 9 Ω (d) zero

[ESE-1999]

4. Transient State Analysis

4.1 On closing switch '*S*', the circuit in the given figure is in steady-state. The current in the inductor after opening the switch '*S*' will



(a) decay exponentially with a time constant of 2s
(b) decay exponentially with a time constant of 0.5s
(c) consist of two decaying exponentials each with a time constant of 0.5s
(d) be oscillatory **[ESE-1999]**

5. Two Port Network Parameters

5.1 Consider the following statements for a 2-port network:

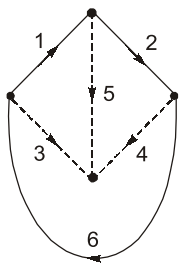
1. $Z_{11} = Z_{22}$ 2. $h_{12} = h_{21}$
3. $Y_{12} = -Y_{21}$ 4. $BC - AD = -1$

The network is reciprocal if and only if
(a) 1 and 2 are correct
(b) 2 and 3 are correct
(c) 3 and 4 are correct
(d) 4 alone is correct

[ESE-1999]

6. Graph Theory & Magnetically Coupled Circuits

6.1 Consider the graph and tree (dotted) of the given figure



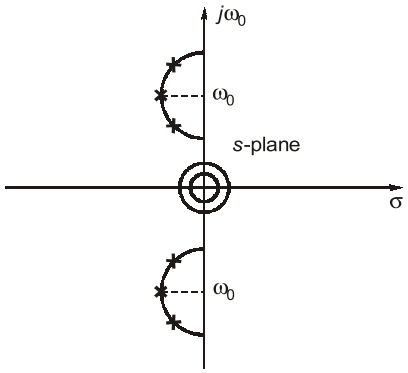
The fundamental loops include the set of lines
(a) (1, 5, 3), (5, 4, 2) and (3, 4, 6)
(b) (1, 2, 4, 3), (1, 2, 6), (3, 4, 6) and (1, 5, 4, 6)
(c) (1, 5, 3), (5, 4, 2), (3, 4, 6) and (2, 4, 3, 1)
(d) (1, 2, 4, 3) and (3, 4, 6)

[ESE-1999]

7. Network Synthesis and Filters

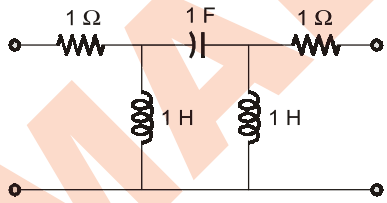
7.1 Voltage transfer function of a simple *RC* integrator has
(a) a finite zero and a pole at infinity
(b) a finite zero and a pole at the origin
(c) a zero at the origin and a finite pole
(d) a zero at infinity and a finite pole
[ESE-1999]

7.2 The given figure shows the pole-zero pattern of a filter in the s-plane. The filter is a



(a) band elimination filter
(b) band-pass filter
(c) low-pass filter
(d) high-pass filter **[ESE-1999]**

7.3 Driving-point impedance of the network shown in the figure is



(a) $\frac{s^3+2s^2+s+1}{2s^2+1}$ (b) $\frac{s^3+s^2+s+1}{s^2+1}$
(c) $\frac{2s^2+1}{s^3+2s^2+s+1}$ (d) $\frac{s^3+2s^2+s+1}{s^2+1}$
[ESE-1999]

7.4 Match the **List-I** (Network) with **List-II** (Poles of driving-point impedance) and select the correct answer using the codes given below the lists:

List-I	List-II
A. *LC*	1. Negative real
B. *RC*	2. Imaginary
C. *RLC*	3. Either real or complex
D. *RL*	

Codes:

	A	B	C	D
(a)	1	2	3	1
(b)	1	2	1	3
(c)	2	1	1	3
(d)	2	1	3	1

[ESE-1999]

7.5 If two identical first order loss-pass filters are cascaded non-interactively, then the unit step response of the composite filter will be
(a) critically damped (b) underdamped
(c) overdamped (d) oscillatory
[ESE-1999]

7.6 Consider the following statements regarding the driving point admittance function.

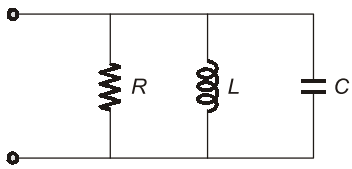
$$Y(s) = \frac{s^2+2.5s+1}{s^2+4s+3}$$

1. It is an admittance of *RL* network.
2. Poles and zeroes alternate on the negative real axis of the s-plane.
3. The lowest critical frequency is a pole.
4. $Y(0) = 1/3$

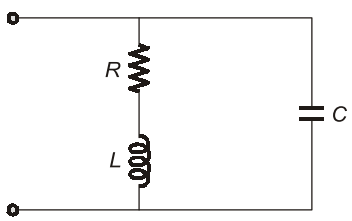
Which of these statements are correct?
(a) 1, 2 and 3 (b) 2 and 4
(c) 1 and 3 (d) 1, 2, 3 and 4
[ESE-1999]

7.7 An *R-L-C* circuit for the driving-point admittance function $\left(\frac{1/RLs}{\frac{1}{R}+\frac{1}{Ls}}+Cs\right)$ is

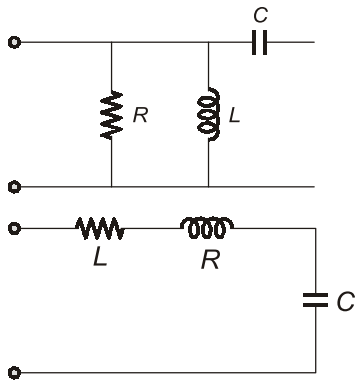
(a)



(b)



(c)



(d)

[ESE-1999]

7.8 Match **List-I** (Form) with **List-II** (Networks) and select the correct answer using the codes given below the lists:

List-I	List-II
A. Cauer I	1. L in series arms and *C* in shunt arms of a ladder
B. Cauer II	2. *C* in series arms and *L* in shunt arms of a ladder
C. Foster I	3. Series combination of *L* and *C* in parallel
D. Foster II	4. Parallel combination of *L* and *C* in series

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	1	2	4	3
(c)	2	1	4	3
(d)	2	1	3	4

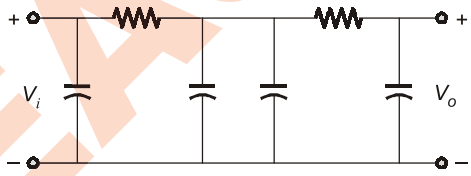
[ESE-1999]

7.9 Poles and zeroes of a driving-point function of a network are simple and interlace on the $j\omega$ axis. The network consists of elements.

(a) *R* and *C* (b) *L* and *C*
(c) *R* and *L* (d) *R*, *L* and *C*

[ESE-1999]

7.10 For the circuit shown in the figure, the order of the differential equation relating V_0 and V_i will be



(a) 4 (b) 3
(c) 2 (d) 1 [ESE-1999]

■■■

Answers Network Theory

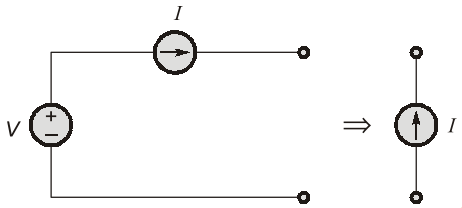
1.1	(b)	1.2	(d)	1.3	(b)	1.4	(b)	1.5	(d)	1.6	(d)	2.1	(a)	2.2	(a)	2.3	(c)
2.4	(a)	2.5	(d)	3.1	(d)	3.2	(c)	3.3	(d)	3.4	(d)	4.1	(b)	5.1	(d)	6.1	(a)
7.1	(d)	7.2	(b)	7.3	(a)	7.4	(d)	7.5	(a)	7.6	(b)	7.7	(b)	7.8	(a)	7.9	(b)
7.10	(b)																

Explanations Network Theory

1. Basics of Network Analysis

1.1 (b)

Ideal current-source in series with any element is redundant



1.2 (d)

From fig. I, $R'_{eq} = \dfrac{1}{\frac{1}{32R}+\frac{1}{16R}+\frac{1}{8R}} = \dfrac{32R}{7}$

From fig. II, $R''_{eq} = \dfrac{1}{\frac{1}{4R}+\frac{1}{2R}+\frac{1}{R}} = \dfrac{4R}{7}$

equating both

$$R'_{eq} = R''_{eq} + R_0$$

$$\Rightarrow \quad R_0 = \frac{32R}{7} - \frac{4R}{7} = \frac{28R}{7} = 4R$$

1.3 (b)

Equivalent *T*-network impedances are

$$R_1 = \frac{24\times16}{24+16+24} = \frac{24\times16}{64} = 6\ \Omega$$

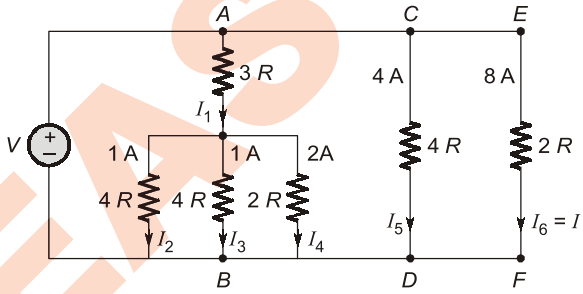
$$R_2 = \frac{24\times16}{24+16+24} = \frac{24\times16}{64} = 6\ \Omega$$

$$R_3 = \frac{24\times24}{24+16+24} = \frac{24\times24}{64} = 9\ \Omega$$

1.4 (b)

The current 'I' is independent of R. So, it will remain 2 A.

1.5 (d)



Given, $I_3 = 1$ A

then $I_2 = 1$ A

$I_4 = 2$ A

Using KCL, $I_1 = 1 + 1 + 2 = 4$ A

Equivalent resistance of branch AB

$$R_{AB} = 3R + 4R \parallel 4R \parallel 2R$$

$$R_{AB} = 4R$$

$$I_5 = I_1 = 4\text{ A} \qquad (\because R_{CD} = R_{AB})$$

then $I_6 = 8\text{ A} = I$

1.6 (d)

Applying KVL,

$-E + Ri + v_c = 0$

But, $i = C\dfrac{dv_c}{dt}$

So, $-E + RC\dfrac{dv_c}{dt} + v_c = 0$

$$\frac{dv_c}{dt} = \frac{E}{RC} - \frac{v_c}{RC}$$

Comparing with the given equation, i.e.

$$\frac{dv_c}{dt} = 1.25v_c + 2$$

$$\frac{1}{RC} = 1.25 \qquad \text{... (i)}$$

$$\frac{E}{RC} = 2 \qquad \text{... (ii)}$$

The values given in sets 2 & 3 satisfy the above equations.

2. Steady State Sinusoidal Analysis & Resonance

2.1 (a)

Inductive reactance,

$$\omega_0 L = 1000\ \Omega$$

Capacitive reactance,

$$\frac{1}{\omega_0 C} = 1000\ \Omega$$

Resistance, $R = 0.1\ \Omega$

Resonant frequency,

$$f_0 = 10\ \text{MHz}$$

$$\text{BW} = \frac{f_0}{Q} = \frac{f_0}{\omega_0 L/R} = \frac{Rf_0}{\omega_0 L}$$

Putting values,

$$\text{BW} = \frac{0.1\times 10\times 10^6}{10^3} = 10^3 = 1\ \text{kHz}$$

Other formula,

$$\text{BW} = \frac{f_0}{Q} = \frac{f_0}{1/\omega_0 CR}$$

$$= \frac{Rf_0}{1/\omega_0 C} = \frac{0.1\times 10\times 10^6}{10^3}$$

$$\text{BW} = 1\ \text{kHz}$$

2.2 (a)

From the figure,

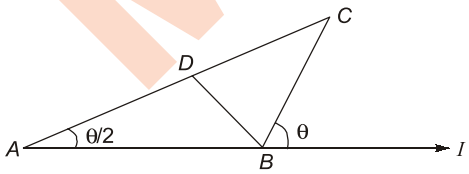
$$V_{AD} = V_{DC}$$

$$\Rightarrow \quad |V_{AD}| = |V_{DC}|$$

Given that

$$|V_{AB}| = |V_{BC}|$$

Drawing the phasor diagram of the given network,



In ΔADB & ΔCDB

$AB = BC \because |V_{AB}| = |V_{BC}|$

$AD = DC \because |V_{AD}| = |V_{DC}|$

$\angle ADB = \angle CDB$ (i.e. 90°)

So, ΔADB & ΔCDB are congruent triangles.

$\therefore \quad \angle ABD = \angle CBD$

But $\angle ABC = 180° - \theta$

$\therefore \quad \angle ABD = (180° - \theta)/2$

$= 90° - \theta/2$

$\therefore \quad \angle BAD = \theta/2$

Now, in ΔABD,

$$\tan\theta/2 = \frac{BD}{AD}$$

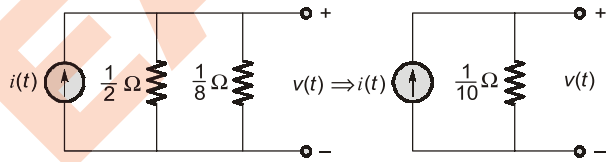
or $$\tan\theta/2 = \frac{|V_{BD}|}{|V|/2} = \frac{2|V_{BD}|}{|V|}$$

or $$\theta/2 = \tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$$

or $$\theta = 2\tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$$

2.3 (c)

The circuit in steady state will be



$$v(t) = 1\times\frac{1}{10} = 0.1\ \text{V}$$

2.4 (a)

$$V_{avg} = \frac{\int_0^{\pi} V\sin(\omega t+\phi)d\omega t}{2\pi}$$

$$= \frac{V}{2\pi}\left[-\cos(\omega t+\phi)\right]_0^{\pi} = \frac{V}{2\pi}\cdot 2\cos\phi$$

$$V_{avg} = \frac{V}{\pi}\cos\phi$$

2.5 (d)

$$V_o = |V_R - V_C|$$

$$V_R = 10\times\frac{R}{2R} = 5\ \text{V}$$

$$V_C = \frac{10\times\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}} = \frac{10}{j\omega CR+1}$$

$$V_o = 5 - \frac{10}{j\omega CR+1}$$

$$V_o = \frac{5j\omega CR+5-10}{j\omega RC+1}$$

$$V_o = \frac{5(j\omega CR - 1)}{j\omega CR + 1}$$

$$|V_o| = \frac{5\sqrt{1^2 + \omega^2 C^2 R^2}}{\sqrt{1^2 + \omega^2 C^2 R^2}} = 5\ \text{V}$$

3. Network Theorems

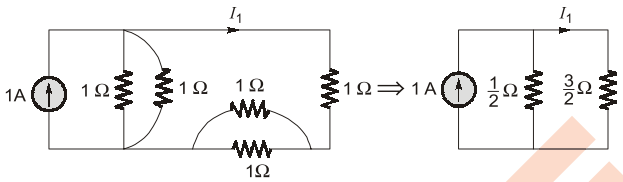
3.1 (d)

Tellegen's theorem states that the sum of power delivered to each branch of any electric network is zero. It is applicable for any lumped network having elements which are linear or non-linear, active or passive, time-varying or time-invariant.

3.2 (c)

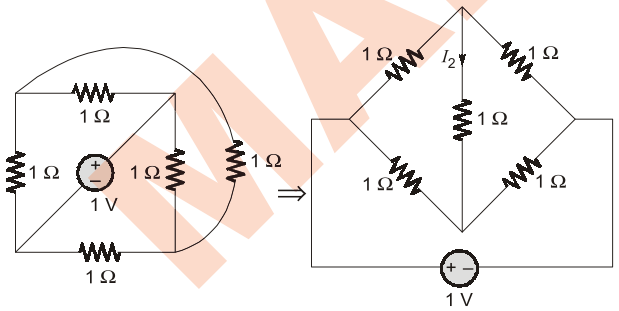
Apply superposition theorem.

First, consider only current source.



$$I_1 = \frac{\frac{1}{2}}{\frac{1}{2} + \frac{3}{2}} \cdot 1 = \frac{1}{4} = 0.25\ \text{A}$$

Now consider only voltage source.



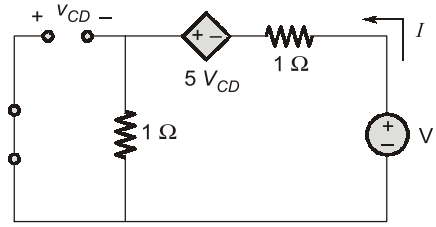
The above circuit is a balanced Wheatstone's bridge. So $I_2 = 0$.

Current flowing through R is $I = I_1 + I_2$

$= 0.25$ A

3.3 (d)

Use $\frac{V}{I} = R_{AB}$



$$V = 1\,I - 5\,V_{CD} + 1\,I \quad \text{...(i)}$$

$$-1\,I = V_{CD} \quad \text{...(ii)}$$

$$V = 1\,I + 5\,I + 1\,I$$

$$\frac{V}{I} = 7\ \Omega = R_{AB}$$

3.4 (d)

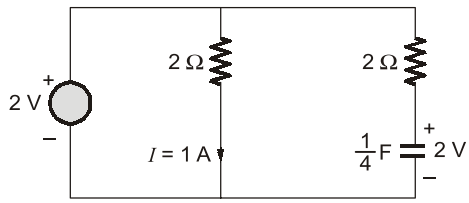
The power dissipated in 30 Ω resistor will be maximum when maximum current will pass through 30 Ω resistor.

For i to be i_{max}, R should be short – circuited, i.e. $R = 0$.

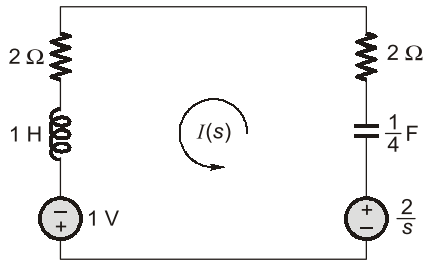
4. Transient State Analysis

4.1 (b)

When the switch 'S' is closed and the circuit is in steady state, the circuit will be as shown below:



Now on opening the switch, the circuit in s-domain will be as shown below:



Applying KVL

$$\frac{4}{s} \cdot I(s) - \frac{2}{s} + 2 \cdot I(s) + 2 \cdot I(s) + s \cdot I(s) - 1 = 0$$

$$\Rightarrow I(s)\left[s + 4 + \frac{4}{s}\right] = 1 + \frac{2}{s}$$

$$\Rightarrow I(s)\left[\frac{s^2+4s+4}{s}\right] = \frac{s+2}{s}$$

$$\Rightarrow \quad I(s) = \frac{1}{s+2}$$

$$\Rightarrow \quad i(t) = e^{-2t}\,\text{A}$$

Comparing with $e^{-t/\tau}$,

$$\tau = \frac{1}{2} = 0.5\ \text{s}.$$

So, the current in the inductor will decay exponentially with a time constant of 0.5 s.

5. Two Port Network Parameters

5.1 (d)

The condition of reciprocity for various parameters is as follows:

Z para $\Rightarrow Z_{12} = Z_{21}$

Y para $\Rightarrow Y_{12} = Y_{21}$

h para $\Rightarrow h_{12} = -h_{21}$

g para $\Rightarrow g_{12} = -g_{21}$

$ABCD$ para $\Rightarrow AD - BC = 1$

$A'\ B'\ C'\ D'$ para $\Rightarrow A'D' - B'C' = 1$

6. Graph Theory & Magnetically Coupled Circuits

6.1 (a)

The number of fundamental loops = $b - n + 1$

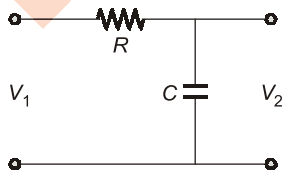
Here, $b = 6$ and $n = 4$.

So number of fundamental loops = 6 – 4 + 1 = 3

7. Network Synthesis and Filters

7.1 (d)

Simple RC integrator circuit is



$$\frac{V_2}{V_1} = \frac{1/Cs}{R + \frac{1}{Cs}} = \frac{1}{1+RCs}$$

It is clear from the above expression that voltage transfer function of a simple RC integrator has a finite pole and a zero at infinity.

7.3 (a)

Driving-point impedance of the network is

$$Z(s) = 1 + \frac{s\left(\frac{1}{s}+s\right)}{s+\frac{1}{s}+s} = \frac{1+s\frac{(s^2+1)}{s}}{\frac{2s^2+1}{s}}$$

$$\Rightarrow \quad Z(s) = 1 + \frac{s^3+s}{2s^2+1}$$

$$= \frac{2s^2+1+s^3+s}{2s^2+1}$$

$$\Rightarrow \quad Z(s) = \frac{s^3+2s^2+s+1}{2s^2+1}$$

7.4 (d)

(i) Form of LC driving point impedance function is $\frac{(s^2+a)(s^2+c)}{s(s^2+b)(s^2+d)}$ where $0 < a < b < c < d$.

It is clear that the poles are at imaginary axis.

(ii) The form of RC driving point impedance function is $\frac{(s+b)(s+d)}{(s+a)(s+c)}$ where $0 < a < b < c < d$.

It is clear that the poles are at negative real axis.

(iii) The form of RL driving point impedance function is $\frac{(s+a)(s+c)}{(s+b)(s+d)}$ where $0 < a < b < c < d$.

It is clear that the poles are at negative real axis.

7.5 (a)

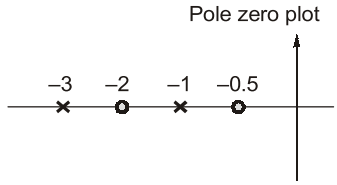
Let the first order response of LPF be $1/(s+\tau)$. Since two identical LPF are cascaded non-interactively, so the unit step response of composite filter will be $1/(s+\tau)^2$, which is critically damped response.

7.6 (b)

$$Y(s) = \frac{s^2+2.5s+1}{s^2+4s+3}$$

$$Y(0) = \frac{1}{3}$$

$$Y(s) = \frac{(s+0.5)(s+2)}{(s+1)(s+3)}$$



⇒ Since, there is a zero nearer to origin, hence lower critical frequency is zero.
So it is *RC* admittance function.

7.7 (b)

Driving point admittance function

$$Y(s) = \frac{1/RLs}{\frac{1}{R}+\frac{1}{Ls}} + Cs$$

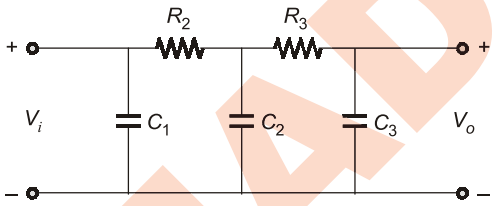
$$= \frac{1/RLs}{\frac{Ls+R}{RLs}} + Cs = \frac{1}{Ls+R} + Cs$$

7.9 (b)

Poles and zeros of the *LC* functions always lie on $j\omega$-axis.
Poles and zeros of *RC* or *RL* functions always lie on negative real axis.

7.10 (b)

The equivalent circuit of the given circuit is shown below:



$$\frac{V_0}{V_i} = \frac{\frac{1}{C_3 s}}{C_1 s + \frac{1}{R_2 + \frac{1}{C_2 s + \frac{1}{R_3 + \frac{1}{C_3 s}}}}}$$

$$\frac{V_0}{V_i} = \frac{\frac{1}{C_3 s}}{C_1 s + \frac{1}{R_2 + \frac{1}{C_2 s + \frac{C_3 s}{R_3 C_3 s + 1}}}}$$

$$= \frac{\frac{1}{C_3 s}}{C_1 s + \frac{1}{R_2 + \frac{R_3 C_3 s + 1}{C_2 s(R_3 C_3 s + 1) + C_3 s}}}$$

$$= \frac{\frac{1}{C_3 s}}{\frac{1}{C_1 s} + \frac{C_2 s(R_3 C_3 s + 1) + C_3 s}{R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1}}$$

$$= \frac{\frac{1}{C_3 s}}{\frac{R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1 + C_1 s\{C_2 s(R_3 C_3 s + 1) + C_3 s\}}{C_1 s\left[R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1\right]}}$$

$$= \frac{As^2 + \ldots.}{Bs^3 + \ldots.}$$ where A and B are constants.

So, the differential equation will be of order of 3.

Note: It can directly be claimed that the order of the differential equation is equal to the number of capacitors in equivalent circuit. In fact, it can be generalized for such type of network.

■■■

2 Electronic Devices and Circuits

1. Semiconductor Physics

1.1 The Ohm's law for conduction in metals is

(a) $J = \sigma E$ (b) $J = E/\sigma$

(c) $J \propto \sigma E$ (d) $J \propto E/\sigma$ **[ESE-1999]**

1.2 **Assertion (A):** In a graded semiconductor, a built-in electric field exists.

Reason (R) : The built-in electric field gives improved performance to a graded base transistor as compared to a uniform base transistor.

(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true

[ESE-1999]

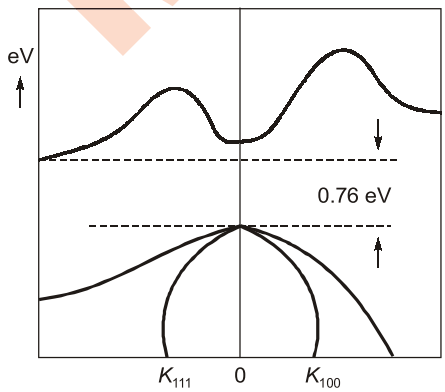
1.3 Quantum effects have to be taken into account in determining the properties of materials if

(a) $E_F = 3/2\ kT$ (b) $E_F < 3/2\ kT$

(c) $E_F > 3/2\ kT$ (d) $E_F >> 3/2\ kT$

[ESE-1999]

1.4# The band structure shown in the given figure is that of



(a) Gallium Arsenide (Ga As)

(b) Silicon (Si)

(c) Copper (Cu)

(d) Germanium (Ge) **[ESE-1999]**

1.5 Which one of the following pairs of semiconductors and current carriers is correctly matched?

(a) Intrinsic : number of electrons = number of holes

(b) *p*-type : number of electrons > number of holes

(c) *n*-type : number of electrons < number of holes

(d) Bulk : Neither electrons nor holes

[ESE-1999]

2. PN-Junction Diodes

2.1 A p-n junction diode's dynamic conductance is directly proportional to

(a) the applied voltage

(b) the temperature

(c) its current

(d) the thermal voltage **[ESE-1999]**

3. Bipolar Junction Transistors

3.1 A transistor with emitter base voltage (V_{EB}) of 20 mV has a collector current (I_C) of 5 mA. For V_{EB} of 30 mV, I_C is 30 mA. If V_{EB} is 40 mV, then the I_C will be

(a) 55 mA (b) 160 mA

(c) 180 mA (d) 270 mA

[ESE-1999]

3.2 Match **List-I** (Devices) with **List-II** (Characteristics) and select the correct answer using the codes given below the lists:

List-I	List-II
A. BJT	1. Voltage controlled –ve resistance
B. MOSFET	2. High current gain
C. Tunnel diode	3. Voltage regulation
D. Zener diode	4. High input impedance

Codes:

	A	B	C	D
(a)	1	4	2	3
(b)	2	4	1	3
(c)	2	3	1	4
(d)	1	3	2	4

[ESE-1999]

3.3 In a junction transistor, the collector cutoff current 'I_{CBO}' reduces considerably by doping the
(a) emitter with high level of impurity
(b) emitter with low level of impurity
(c) collector with high level of impurity
(d) collector with low level of impurity

[ESE-1999]

3.4 In a junction transistor biased for operation at emitter current 'I_E' and collector current 'I_C', the transconductance 'g_m' is
(a) kT/qI_E (b) $qI_E/\bar{k}T$
(c) I_C/I_E (d) I_E/I_C

[ESE-1999]

4. Field Effect Transistors

4.1 The transconductance 'g_m' of a JFET is equal to

(a) $-\frac{2I_{DSS}}{V_P}$ (b) $\frac{2}{|V_P|}\sqrt{I_{DSS}I_{DS}}$

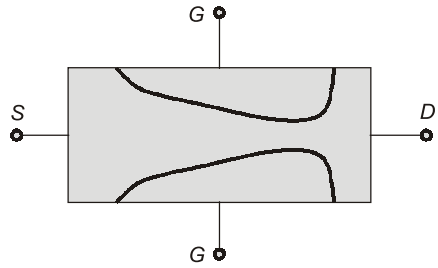
(c) $-\frac{2I_{DS}}{V_P}$ (d) $\frac{I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$

[ESE-1999]

4.2 **Assertion (A):** FETs are more suitable at the input stages of millivoltmeter and CROs than BJTs.
Reason (R): A FET has lower output impedance than a BJT.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

4.3 In a biased JFET, the shape of the channel is as shown in the given figure



because
(a) it is the property of the material used
(b) the drain end is more reverse biased than source end
(c) the drain end is more forward biased than source end
(d) the impurity profile varies with the distance from source

[ESE-1999]

5. Special Diodes and Optoelectronic Devices

5.1 Consider the following statements:
He-Ne LASER
1. gives continuous output
2. emits red light
3. requires a DC magnet
4. can be voice modulated by using a Kerr cell

Which of these statements are correct?
(a) 1, 2 and 3 (b) 1, 3 and 4
(c) 1, 2, and 4 (d) 2, 3 and 4

[ESE-1999]

6. Power Switching Devices

6.1 Which one of the following devices is NOT used as the controller in a stabilizer?
(a) Diac (b) Triac
(c) SCR (d) Power transistor

[ESE-1999]

6.2 SCR turns OFF from conducting state to blocking state on
(a) reducing gate current
(b) reversing gate voltage
(c) reducing anode current below holding current value
(d) applying a.c. to the gate [ESE-1999]

Answers Electronic Devices and Circuits

1.1	(a)	1.2	(b)	1.3	(d)	1.4	(a)	1.5	(a)	2.1	(c)	3.1	(c)	3.2	(b)	3.3	(a)		
3.4	(b)	4.1	(b)	4.2	(a)	4.3	(b)	5.1	(c)	6.1	(a)	6.2	(c)						

Explanations Electronic Devices and Circuits

1. Semiconductor Physics

1.1 (a)

The Ohm's law for conduction in metals is

$$J = \sigma E$$

We have $I = J \cdot A$

$$= \sigma E \cdot A$$

$$= \left(\sigma \frac{V}{l}\right) A = \frac{V}{R} \quad \text{where} \left(R = \frac{l}{\sigma A}\right)$$

where, $l \rightarrow$ length of the conductor

$A \rightarrow$ area of cross-section

$V \rightarrow$ voltage applied

1.2 (b)

In a graded semiconductor, as a result of the non-uniform doping, an electric field is generated within the semiconductor.

1.4 (a)

The band structure shown is of a material having direct bandgap energy and GaAs is a direct bandgap material.

1.5 (a)

In intrinsic semiconductor,
number of electrons = number of holes

2. PN-Junction Diodes

2.1 (c)

p-n junction diode's dynamic conductance

$$g_m \approx \frac{I}{\eta V_T} \text{ or } g_m \propto I.$$

3. Bipolar Junction Transistors

3.1 (c)

We know that $I_c = I_0 e^{+\frac{V_{EB}}{V_T}}$

$$5 = I_0 e^{\frac{20}{V_T}} \quad \text{...(i)}$$

and, $$30 = I_0 e^{\frac{30}{V_T}} \quad \text{...(ii)}$$

from equations (i) & (ii)

$$e^{\frac{10}{V_T}} = 6$$

So $$I_0 = \frac{5}{36} \text{mA} \quad \text{from equation (i)}$$

So $$I_c = I_0 e^{\frac{40}{V_T}}$$

$$I_c = \frac{5}{36} \cdot 6^4 = 180 \text{ mA}$$

3.2 (b)

(i) Zener diode is used for voltage regulation.
(ii) MOSFET has very high input impedance.
(iii) The tunnel diode exhibits a negative-resistance characteristic between the peak current I_P and the minimum value, I_V, called the valley current.

3.3 (a)

By doping the emitter with high level of impurity, the large-signal current gain of a common-base transistor, α increases. But

$$\alpha = \frac{I_C - I_{CBO}}{I_E}$$

Therefore, I_{CBO} reduces on increasing α.

3.4 (b)

$$g_m = \frac{\alpha_0}{r_e}$$

where, $\alpha_0 \rightarrow$ large-signal current gain of a common-base transistor

$r_e \rightarrow$ emitter diode resistance

$r_e = \dfrac{V_T}{I_E}$ where $V_T = \dfrac{kT}{q}$

$\therefore \quad g_m = \dfrac{\alpha_0 I_E q}{kT}$

$\because \quad \alpha_0 \approx 1$

$\therefore \quad g_m \approx \dfrac{q I_E}{kT}$

4. Field Effect Transistors

4.1 (b)

The transconductance of a JFET,

$$g_m = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

where g_{m_0} is the value of g_m for $V_{GS} = 0$, and is given by

$$g_{m_0} = \frac{-2 I_{DSS}}{V_P}$$

Also, $$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

So, $$g_m = \frac{-2 I_{DSS}}{V_P} \cdot \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

or $$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} I_{DS}}$$

6. Power Switching Devices

6.1 (a)

Diac does not have a controlling signal.

6.2 (c)

The holding current may be defined as the minimum value of anode current below which it must fall for turning off the SCR.

■■■

3 Analog Circuits

1. Diodes Circuits

1.1 The ratio of available power from the DC component of a full-wave rectified sinusoid to the available power of the rectified sinusoid is

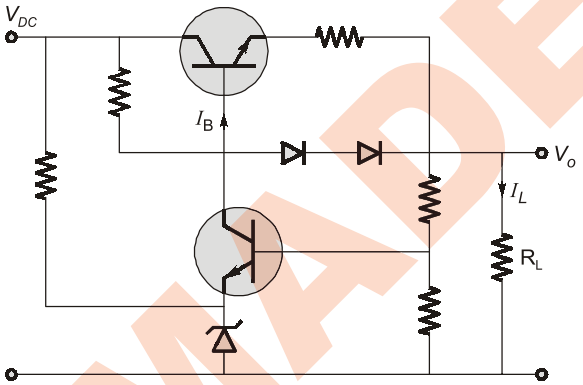
(a) $8/\pi$ (b) 2

(c) $4/\pi$ (d) $8/\pi^2$ **[ESE-1999]**

2. BJT Circuits

2.1 **Assertion (A):** In the circuit shown in the figure, a prescribed value of load current I_L, V_0 will gradually fall.

Reason (R): Above the prescribed value, as load current I_L increases, I_B decreases.



(a) Both A and R are true and R is the correct explanation of A

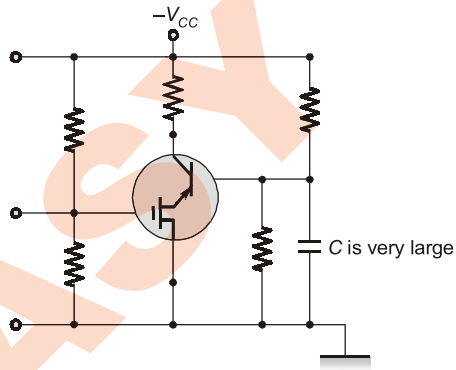
(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true

[ESE-1999]

2.2 The given figure shows a composite transistor consisting of a MOSFET and a bipolar transistor in cascode



The MOSFET has a transconductance g_m of 2 mA/V and the bipolar transistor has $\beta(\triangleq h_{fe})$ of 99. The overall transconductance of the composite transistor is

(a) 198 mA/V (b) 19.8 mA/V

(c) 1.98 A/V (d) 1.98 mA/V

[ESE-1999]

2.3 The input resistance of a common emitter stage can be increased by

1. unbypassing emitter resistance
2. bootstrapping
3. biasing it at low quiescent current
4. using compounded BJTs

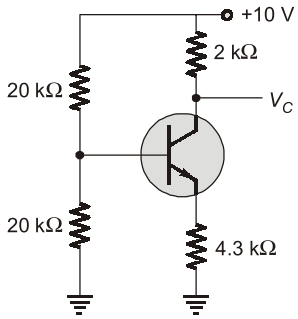
The correct sequence in descending order of the effectiveness of these methods is

(a) 2, 4, 1, 3 (b) 4, 3, 2, 1

(c) 2, 4, 3, 1 (d) 4, 2, 3, 1

[ESE-1999]

2.4 The collector voltage V_C of the circuit shown in the given figure is approximately

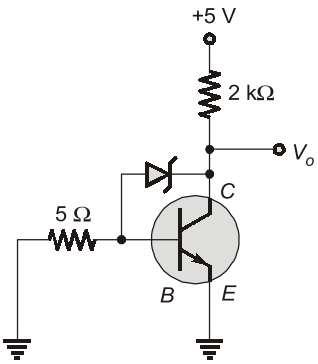


(a) 2 V (b) 4.6 V
(c) 8 V (d) 8.6 V [ESE-1999]

2.5 Consider the following devices:
1. BJT in CB mode
2. BJT in CE mode
3. JFET
4. MOSFET

The correct sequence of these devices in increasing order of their input impedance is
(a) 1, 2, 3, 4 (b) 2, 1, 3, 4
(c) 2, 1, 4, 3 (d) 1, 3, 2, 4 [ESE-1999]

2.6 The voltage V_0 of the circuit shown in the given figure is



(a) 5 V (b) 3.1 V
(c) 2.5 V (d) zero [ESE-1999]

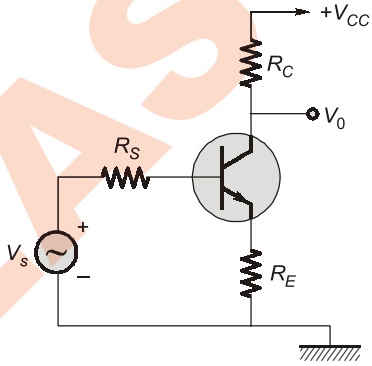
4. Frequency Response of Amplifiers & Filters

4.1 A second-order band-pass active filter can be obtained by cascading a low-pass second-order section having cut-off frequency f_{OH} with a high-pass second-order section having cut-off frequency f_{OL}, provided
(a) $f_{OH} > f_{OL}$ (b) $f_{OH} < f_{OL}$
(c) $f_{OH} = f_{OL}$ (d) $f_{OH} \leq 1/2\ f_{OL}$
[ESE-1999]

5. Feedback Amplifiers

5.1 **Assertion (A):** A large negative feedback is deliberately introduced in an amplifier to make its gain independent of the variation of parameters of the active device and other circuit components.
Reason (R): A large negative feedback results in a high value of return difference compared to unity, which makes the feedback gain inversely proportional to the feedback factor.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-1999]

5.2 The given circuit has a feedback factor of



(a) $-R_C / R_S$ (b) $-R_E / R_C$
(c) $-R_E / R_S$ (d) $-R_C / R_E$
[ESE-1999]

6. Oscillators

6.1 **Assertion (A):** Miller sweep circuit producing sawtooth waveform is a relaxation oscillator.
Reason (R): The active device alternately supplies power to the load and relaxes when it is cut-off.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-1999]

6.2 A Hartley oscillator is used for generating
(a) very low frequency oscillation
(b) radio-frequency oscillation
(c) microwave oscillation
(d) audio-frequency oscillation
[ESE-1999]

7. Operational Amplifiers

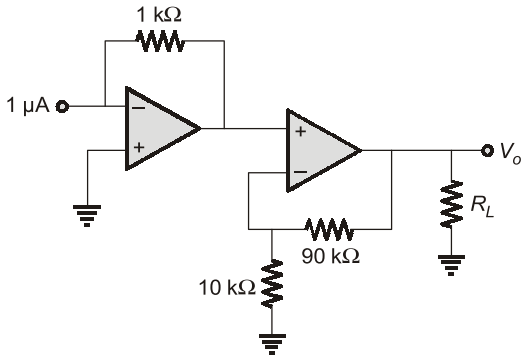
7.1 In a single-stage differential amplifier, the output offset voltage is basically dependent on the mismatch of

(a) V_{BE}, I_B and β (b) V_{BE} and I_B

(c) I_B and β (d) V_{BE} and β

[ESE-1999]

7.2 The output voltage V_0 of the given circuit

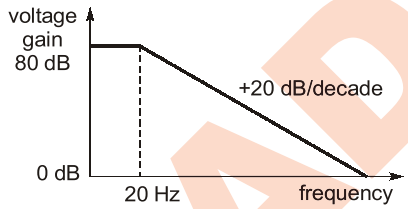


(a) –100 V (b) –100 mV

(c) 10 V (d) –10 mV

[ESE-1999]

7.3 The voltage gain versus frequency curve of an Op-Amp is shown in the given figure



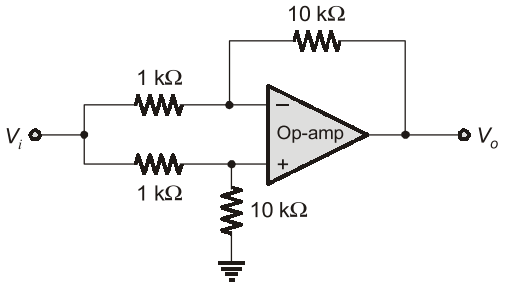
The gain-bandwidth product of the Op-Amp is

(a) 200 Hz (b) 200 MHz

(c) 200 kHz (d) 2 MHz

[ESE-1999]

7.4 The V_0 of the Op-Amp circuit shown in the given figure is



(a) 11 V_i (b) 10 V_i

(c) V_i (d) zero [ESE-1999]

8. Power Amplifiers and Regulators

8.1 If a class *C* power amplifier has an input signal with frequency of 200 kHz and the width of collector current pulses of 0.1 μs, then the duty cycle of the amplifier will be

(a) 1 % (b) 2 %

(c) 10 % (d) 20 %

[ESE-1999]

8.2 Thermal runaway will take place if the quiescent point is such that

(a) $V_{CE} > 1/2\ V_{CC}$ (b) $V_{CE} < V_{CC}$

(c) $V_{CE} < 2\ V_{CC}$ (d) $V_{CE} < 1/2\ V_{CC}$

[ESE-1999]

8.3 To avoid thermal runway in the design of an analog circuit, the operating point of the BJT should be such that it satisfies the condition

(a) $V_{CE} = V_{CE}/2$ (b) $V_{CE} \leq V_{CE}/2$

(c) $V_{CE} > V_{CE}/2$ (d) $V_{CE} \leq 0.78\ V_{CE}$

[ESE-1999]

8.4 The unit of a thermal resistance of a semiconductor device is

(a) Ohms (b) Ohms/°C

(c) °C/Ohm (d) °C/Watt

[ESE-1999]

8.5 In a feedback series regulator circuit, the output voltage is regulated by controlling the

(a) magnitude of the input voltage

(b) gain of the feedback transistor

(c) reference voltage

(d) voltage drop across the series pass transistor

[ESE-1999]

8.6 A three-terminal monolithic IC regulator can be used as

(a) an adjustable output voltage regulator alone

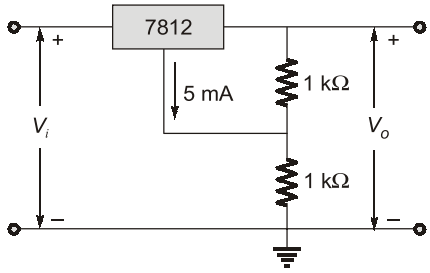
(b) an adjustable output voltage regulator and a current regulator

(c) a current regulator and a power switch

(d) a current regulator alone

[ESE-1999]

8.7 A 12 V monolithic regulator is adjusted to obtain a higher output voltage as shown in the given figure



The V_0 will be

(a) 12 V (b) 17 V

(c) 24 V (d) 29 V [ESE-1999]

9. Multivibrators and Timers

9.1 **Assertion (A):** A monostable multivibrator can be used to alter the pulse width of a repetitive pulse train.

Reason (R): Monostable multivibrator has a single stable state.

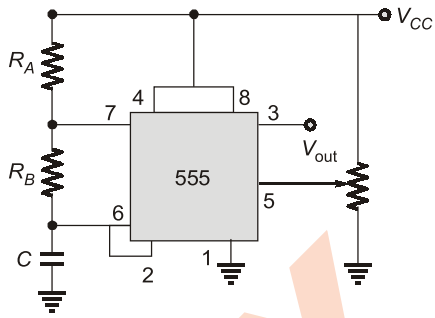
(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true [ESE-1999]

9.2 Circuit shown in the given figure represents



(a) an astable multivibrator

(b) a monostable multivibrator

(c) voltage-controlled oscillator

(d) ramp generator [ESE-1999]

■■■

Answers Analog Circuits

1.1	(d)	2.1	(c)	2.2	(d)	2.3	(d)	2.4	(c)	2.5	(a)	2.6	(*)	4.1	(a)	5.1	(a)		
5.2	(b)	6.1	(d)	6.2	(b)	7.1	(c)	7.2	(d)	7.3	(c)	7.4	(d)	8.1	(b)	8.2	(a)		
8.3	(b)	8.4	(d)	8.5	(d)	8.6	(a)	8.7	(d)	9.1	(b)	9.2	(c)						

Explanations Analog Circuits

1. Diodes Circuits

1.1 (d)

For full wave rectifier,

$$I_{dc} = \frac{2I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\frac{P_{dc}}{P} = \frac{(I_{dc})^2 R}{(I_{rms})^2 R} = \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} = \frac{8}{\pi^2}$$

2. BJT Circuits

2.2 (d)

$$g_m = \frac{I_D}{V_i}$$

In the figure, $I_E = I_D$ and $I_C = \alpha I_E$

$$g_{m_{overall}} = \frac{I_c}{V_i} = \frac{\alpha I_E}{V_i} = \frac{\alpha I_D}{V_i} = \alpha g_m$$

$$\Rightarrow \quad g_{m_{overall}} = \frac{\beta}{\beta+1} \cdot g_m = \frac{99}{99+1} \times 2$$

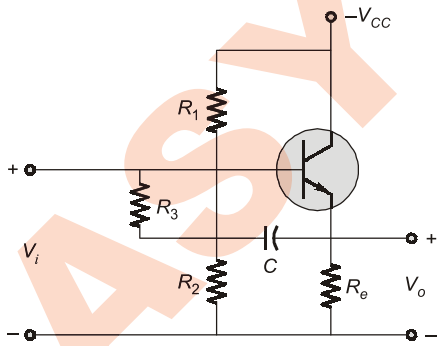
$$= 1.98 \text{ mA/V}$$

2.3 (d)

In bootstrapping, $A_v \to 1$, and effective input resistance becomes extremely large as

$$R_{eff} = \frac{R_3}{1 - A_v}$$

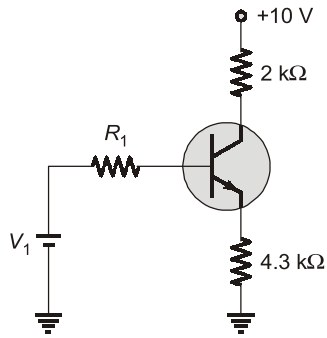
Thus the most effective way to increase the input resistance is through bootstrapping and the least effective way is to reduce the bias current.



2.4 (c)

$$V_1 = \frac{20}{20+20} \times 10 = 5 \text{ V}$$

$$R_1 = \frac{20 \times 20}{20+20} = 10 \text{ k}\Omega$$



KVL:

$$V_1 = R_1 I_B + V_{BE} + 4.3 I_E$$

Let $\beta > 1$. So $I_B \approx 0$ & $I_E \approx I_C$

$$V_1 = V_{BE} + 4.3 I_C$$

$$\Rightarrow \quad 5 - 0.7 = 4.3 I_C$$

$$\Rightarrow \quad I_C = 1 \text{ mA}$$

$$V_C = 10 - 2 \times 1$$

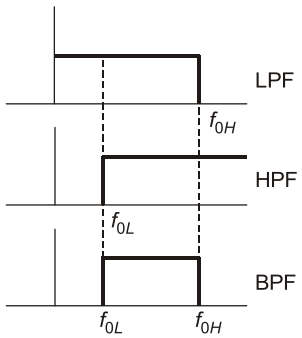
$$\Rightarrow \quad V_C = 8 \text{ V}$$

2.5 (a)

The increasing order of impedance is given below:
BJT (CB) < BJT (CE) < JFET < MOSFET.

4. Frequency Response of Amplifiers & Filters

4.1 (a)



It is clear from the diagram that to make a bandpass filter $f_{0H} > f_{0L}$

5. Feedback Amplifiers

5.1 (a)

$$A_{v_f} = \frac{A_v}{1 + A_v\beta}$$

when $\beta >> 1$, $A_{v_f} \cong \frac{A_v}{A_v\beta} = \frac{1}{\beta}$

Thus, gain A_{v_f} is independent of A_v.

Note: Return difference, $D = 1 + A_v\beta$.

5.2 (b)

$$\beta = \frac{V_f}{V_0} = \frac{-I_C R_E}{I_C R_C} = \frac{-R_E}{R_C}$$

6. Oscillators

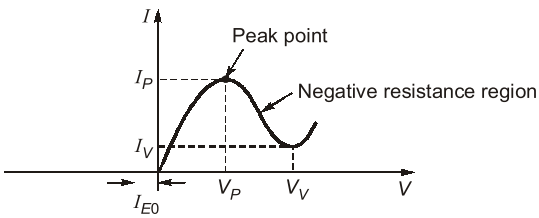
6.2 (b)

RF oscillators ($f > 20$ kHz) — Hartley, Colpitt, Clapp, Crystal

AF oscillators ($f < 20$ kHz) — RC phase shift, Wein bridge

6.4 (a)

UJT characteristic curve:



7. Operational Amplifiers

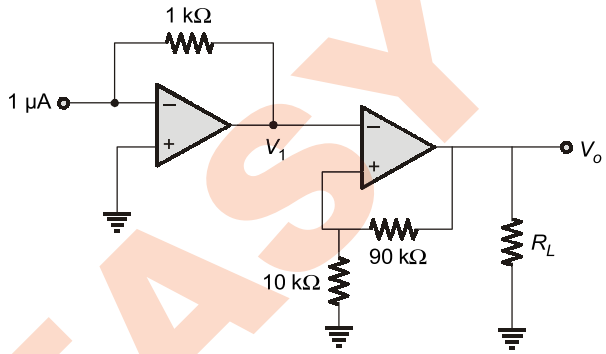
7.1 (c)

The output offset voltage

$$V_{OOV} = (A_{OO})V_{iO} + R_F I_B$$

where A_{OO} depends on β and I_B.

7.2 (d)



$$V_1 = \frac{10}{10+90} \cdot V_0$$

$$\Rightarrow \quad V_1 = \frac{V_0}{10}$$

$$V_1 = -1 \times 10^3 \times 1 \times 10^{-6}$$

$$\Rightarrow \quad \frac{V_0}{10} = -10^{-3}$$

$$\Rightarrow \quad V_0 = -10 \text{ mV}$$

7.3 (c)

$$80 \text{ dB} = 20 \log A_v$$

$$\Rightarrow \quad A_v = 10^4$$

GBW product $= 10^4 \times 20 = 200$ kHz

7.4 (d)

$$V_0 = -\frac{10}{1} \cdot V_i + V_i\left(\frac{10}{10+1}\right)\left(1+\frac{10}{1}\right)$$

$$\Rightarrow \quad V_0 = -10V_i + 10V_i\left(\frac{10}{11}\right)(11)$$

$$\Rightarrow \quad V_0 = -10\ V_i + 10\ V_i = 0$$

8. Power Amplifiers and Regulators

8.1 (b)

Time period,

$$T = \frac{1}{f} = \frac{1}{200 \times 10^3} = 5 \times 10^{-6} = 5\,\mu\text{sec}$$

Pulse width $\tau = 0.1\ \mu$ sec

$$\text{Duty cycle} = \frac{\tau}{T} \times 100 = \frac{0.1}{5} \times 100 = 2\%$$

8.2 **(a)**

To avoid thermal runway,

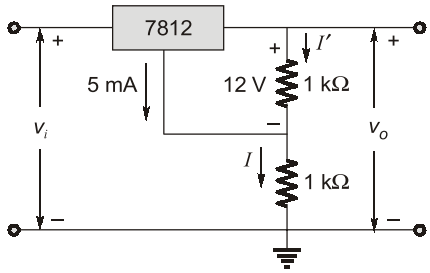
$$V_{CE} < \frac{V_{CC}}{2}$$

8.3 **(b)**

To avoid thermal runaway,

$$V_{CE} < V_{CC}/2$$

8.7 **(d)**



Output of IC 7812 is + 12 V.

$$I' = \frac{12}{1\text{k}\Omega} = 12\,\text{mA}$$

Using KCL

$\therefore \quad I = 5 + I' = 17$ mA

So $\quad V_o = 12 + 1 \times 17 = 29$ V

9. Multivibrators and Timers

9.1 **(b)**

Monostable multivibrator is used as pulse stretcher.

■■■

4 Digital Circuits

2. Boolean Algebra

2.1 The Boolean theorem $AB + \bar{A}C + BC = AB + \bar{A}C$ corresponds to

(a) $(A + B).(\bar{A} + C).(B + C) = (A + B).(\bar{A} + C)$

(b) $AB + \bar{A}C + BC = AB + BC$

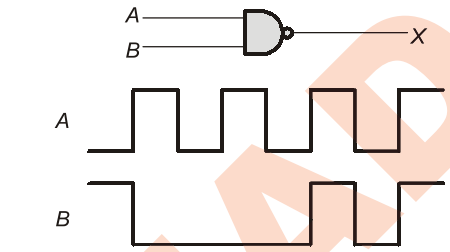
(c) $AB + \bar{A}C + BC = (A + B)(\bar{A} + C)(B + C)$

(d) $(A + B)(\bar{A} + C)(B + C) = AB + \bar{A}C$

[ESE-1999]

3. Logic Gates

3.1 The given figure shows a NAND gate with input waveforms A and B



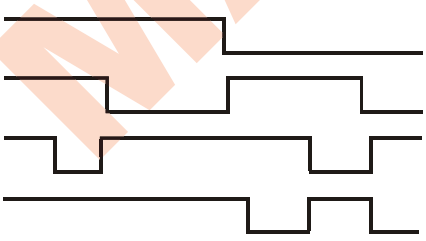
The correct output waveform X of the gate is

(a)

(b)

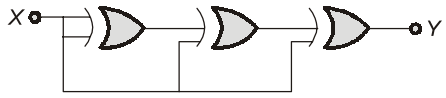
(c)

(d)



[ESE-1999]

3.2 The output Y of the given circuit is



(a) 1 (b) zero

(c) X (d) $\bar{X}$ **[ESE-1999]**

3.3 $Y = f(A, B) = \Pi M\,(0, 1, 2, 3)$ represents (M is Maxterm)

(a) NOR gate

(b) NAND gate

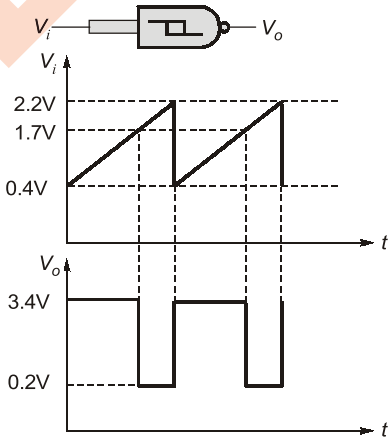
(c) OR gate

(d) a situation where output is independent of input

[ESE-1999]

3.4 The input waveform V_i and the output wave-form V_0 of a Schmitt NAND are shown in the given figures.

The duty cycle of the output waveform will be



(a) 100% (b) 85.5%

(c) 72.2% (d) 25% **[ESE-1999]**

4. Combinational Circuits

4.1 **Assertion (A):** A demultiplexer can be used as a decoder.

Reason (R): A demultiplexer is built by using AND gates only.

(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true **[ESE-1999]**

4.2 Match **List-I** (Circuits) with **List-II** (Types of integration level) and select the correct answer using the codes given below the lists:

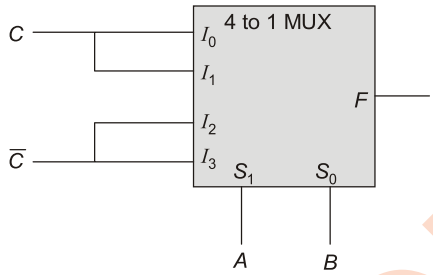
List-I	List-II
A. Full adder	1. VLSI
B. Magnitude comparator	2. SSI
C. Programmable logic array	3. MSI

Codes:

	A	B	C
(a)	2	3	1
(b)	3	2	1
(c)	1	3	2
(d)	2	1	3

[ESE-1999]

4.3 The logic circuit realized by the circuit shown in the given figure will be



(a) $B \odot C$ (b) $F = B \oplus C$
(c) $A \odot C$ (d) $F = A \oplus C$

[ESE-1999]

5. Sequential Circuits

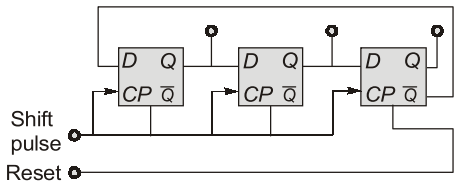
5.1 In a negative edge triggered *J-K* flip-flop, in order to have the output *Q* state 0, 0 and 1 in the next three successive clock pulses, the *J-K* input states required would be respectively
(a) 00, 00 and 10 (b) 00, 01 and 11
(c) 00, 10 and 11 (d) 01, 10 and 11

[ESE-1999]

5.2 The initial state of *MOD*-16 down counter is 0110. After 37 clock pulses, the state of the counter will be
(a) 1011 (b) 0110
(c) 0101 (d) 0001

[ESE-1999]

5.3 A three-bit shift register is shown in the given figure



To have the content '000' again, the number of clock pulses required would be
(a) 3 (b) 6
(c) 8 (d) 16 **[ESE-1999]**

5.4 Symmetrical square wave of time period 100 μs can be obtained from square wave of time period 10 μs by using a
(a) divide by-5 circuit
(b) divide by-2 circuit
(c) divide by-5 circuit followed by a divide by-2 circuit
(d) *BCD* counter **[ESE-1999]**

5.5 A 1 μs pulse can be converted into a 1ms pulse by using
(a) a monostable multivibrator
(b) an astable multivibrator
(c) a bistable multivibrator
(d) a *J-K* flip-flop **[ESE-1999]**

6. Memories and Programmable Logic Devices

6.1 For a particular type of memory, the access time and the cycle time are respectively 200 ns and 200 ns. The maximum rate at which the data can be accessed, is
(a) 2.5×10^6 /s (b) 5×10^6 /s
(c) 0.2×10^6 /s (d) 10^6 /s

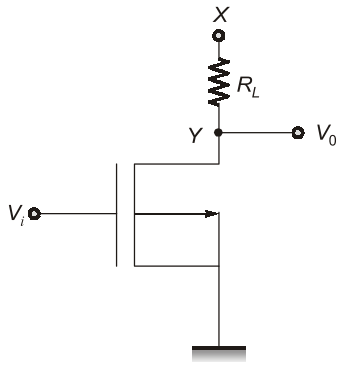
[ESE-1999]

7. Logic Families

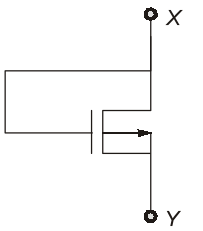
7.1 The voltage levels of a negative logic system
(a) must necessarily be negative
(b) may be negative or positive
(c) must necessarily be positive
(d) must necessarily be 0 V and –5 V

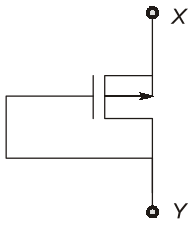
[ESE-1999]

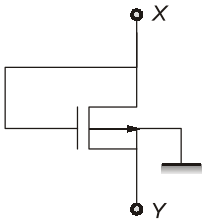
7.2 The load resistance R_L between X and Y in the switch shown in Figure-I

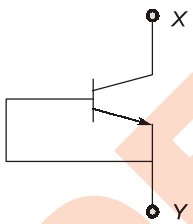


CANNOT be replaced by

(a)


(b)


(c)


(d)


[ESE-1999]

7.3 Consider the following statements regarding *IC*s:
1. ECL has the least propagation delay.
2. TTL has the largest fanout.
3. CMOS has the biggest noise margin.
4. TTL has the lowest power consumption.

Which of these statements are correct?
(a) 1 and 3 (b) 2 and 4
(c) 3 and 4 (d) 1 and 2

[ESE-1999]

7.4 For a logic family
V_{OH} is the minimum output high level voltage
V_{OL} is the maximum output low level voltage
V_{IH} is the minimum acceptable input high level voltage
V_{IL} is the maximum acceptable input low level voltage
The correct relationship among these is
(a) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$
(b) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$
(c) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$
(d) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$

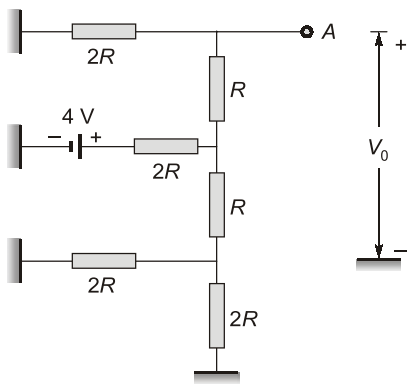
[ESE-1999]

8. ADC and DAC

8.1 **Assertion (A):** The output of an 8-bit A to D converter is 80H for an input of 2.5 V.
Reason (R): ADC has an output range of 00 to FFH for an input range of –5 V to + 5 V.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

8.2 The output voltage V_0 with respect to ground of the R-$2R$ ladder network shown in the given figure is



(a) 1 V (b) 2 V
(c) 3 V (d) 4 V [ESE-1999]

■■■

Answers Digital Circuits

2.1	(a)	**3.1**	(d)	**3.2**	(b)	**3.3**	(d)	**3.4**	(c)	**4.1**	(b)	**4.2**	(b)	**4.3**	(d)	**5.1**	(a, b)		
5.2	(d)	**5.3**	(b)	**5.4**	(c)	**5.5**	(a)	**6.1**	(d)	**7.1**	(b)	**7.2**	(d)	**7.3**	(a)	**7.4**	(b)		
8.1	(d)	**8.2**	(a)																

Explanations Digital Circuits

2. Boolean Algebra

2.1 (a)

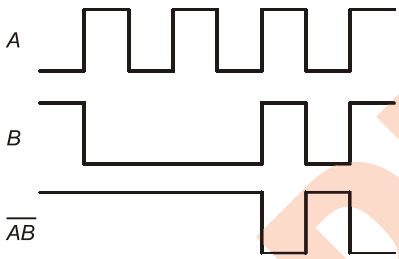
$AB + \bar{A}C + BC = AB + \bar{A}C$

Taking dual of the given equation

$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$

3. Logic Gates

3.1 (d)



3.2 (b)

$Y = X \oplus [X \oplus \{X \oplus X\}]$

$\Rightarrow \quad Y = X \oplus [X \oplus 0]$

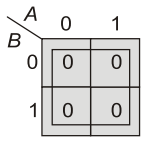
$\Rightarrow \quad Y = X \oplus X$

$\Rightarrow \quad Y = 0$

3.3 (d)

$Y = f(A, B) = \Pi M(0, 1, 2, 3)$

K-map for Y:



If all the cells in a maxterms K-map are grouped, this means that the output y is equal to 0 for every possible input.

$y = 0$ which represents a situation where output is independent of input.

3.4 (c)

$$\text{Duty cycle} = \frac{T_{on}}{T} \times 100$$

$$= \frac{(1.7 - 0.4)}{(2.2 - 0.4)} \times 100 \times 100$$

$$= 72.2\%$$

4. Combinational Circuits

4.3 (d)

$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

$\Rightarrow \quad F = \bar{A}C(\bar{B} + B) + A\bar{C}(\bar{B} + B)$

$\Rightarrow \quad F = \bar{A}C + A\bar{C}$

$\because \quad \bar{B} + B = 1$

$\Rightarrow \quad F = A \oplus C$

5. Sequential Circuits

5.1 (a, b)

Characteristic Table for JK flip-flop is

J	K	$Q(t+1)$	
0	0	$Q(t)$	Hold state
0	1	0	Reset state
1	0	1	Set state
1	1	$\overline{Q(t)}$	Toggle state

5.2 (d)

$37 = 16 \times 2 + 5$

After 37 clock pulses, the state of MOD-16 DOWN counter will be five states below the present state.

$$\begin{array}{r} 0110 \\ -0101 \\ \hline 0001 \end{array}.$$

5.3 (b)

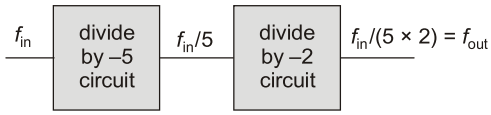
The given circuit is a switch-tail ring counter or Johnson counter in which n flip-flops provide 2n distinguishable states. Therefore, 3 flip-flops will provide 6 states.

5.4 (c)

Output frequency $f_{out} = \dfrac{1}{100\ \mu s}$

Input frequency $f_{in} = \dfrac{1}{10\ \mu s}$

$f_{out} = \dfrac{f_{in}}{10}$



5.5 (a)

A monostable multivibrator is used as a pulse stretcher.

7. Logic Families

7.1 (b)

The voltage levels of a negative logic system may be negative or positive provided voltage level of logic 1 < voltage level of logic 0.

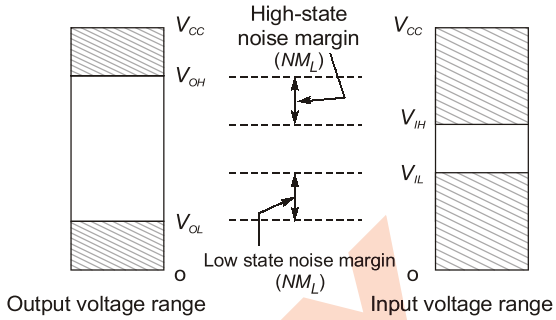
7.2 (d)

One advantage of the MOS device is that it can be used not only as a switch, but as a resistor as well. A resistor is obtained from the MOS by permanently biasing the gate terminal for conduction, the resistance of the conduction channel thus created effectively acts as load resistance. In MOS, channel resistance, $R \propto \dfrac{1}{W/L}$ where W and L are the width and length of the channel respectively.

7.3 (a)

(i) CMOS has the largest fan-out.
(ii) CMOS has the lowest power consumption.

7.4 (b)



8. ADC and DAC

8.1 (d)

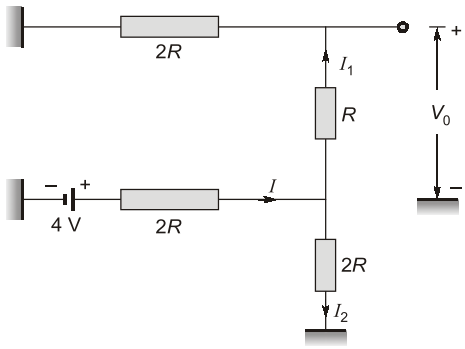
$(FFH)_{16} = (255)_{10}$
$(80H)_{16} = (128)_{10}$

Input for the output of 80H is

$-5 + \dfrac{128}{255} \times [5 - (-5)]$, i.e. 0 V.

8.2 (a)

The equivalent circuit is shown:



$2R.I + (R + 2R).I_1 = 4$

$I_1 + I_2 = I$ and $3I_1 = 2I_2$

$\Rightarrow \quad I_1 + \dfrac{3}{2} I_1 = I$

$\Rightarrow \quad I = 2.5\, I_1$

$\Rightarrow \quad 2R(2.5I_1) + 3RI_1 = 4$

$\Rightarrow \quad 8RI_1 = 4$

$\Rightarrow \quad I_1 = \dfrac{4}{8R} = \dfrac{1}{2R}$

$\Rightarrow \quad V_0 = 2R.I_1$

$= 2R \cdot \dfrac{1}{2R} = 1$ V

5 Materials Science

2. Dielectric and Ceramic Materials

2.1 Consider the following statements regarding an insulating material connected to an a.c. signal:
1. The dielectric constant increases with frequency
2. The dielectric constant decreases with frequency
3. Atomic polarization decreases with frequency

Which of these statement(s) is/are correct?
(a) 3 alone (b) 2 alone
(c) 2 and 3 (d) 1 and 3

[ESE-1999]

2.2 The most important set of specifications of transformer oil includes
(a) dielectric strength and viscosity
(b) dielectric strength and flash point
(c) flash point and viscosity
(d) dielectric strength, flash point and viscosity

[ESE-1999]

2.3 **Assertion (A) :** A uniaxial stress on the ends of a piezoelectric crystal develops a potential difference between the two ends of the crystal.
Reason (R) : The ions in the crystal get displaced and produce dipoles.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

3. Magnetic Materials

3.1 The magnetic moment in units of Bohr magnetron of a ferrous ion in any ferrite is
(a) zero (b) 2
(c) 4 (d) 6

[ESE-1999]

3.2 For a permanent magnetic material
(a) the residual induction and the coercive field should be large
(b) the residual induction and the coercive field should be small
(c) the area of hysteresis loop should be small
(d) the initial relative permeability should be large

[ESE-1999]

4. Conductors and Superconductors

4.1 The magnetization 'M' of a superconductor in a field of H is
(a) extremely small (b) $-H$
(c) -1 (d) zero [ESE-1999]

4.2 The maximum power handling capacity of a resistor depends on
(a) total surface area
(b) resistance value
(c) thermal capacity of the resistor
(d) resistivity of the material used in the resistor

[ESE-1999]

■■■

Answers Materials Science

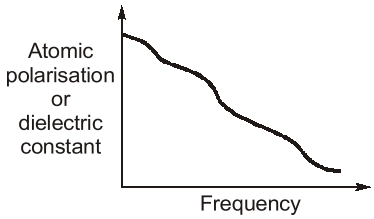
2.1 (c) **2.2** (d) **2.3** (a) **3.1** (c) **3.2** (a) **4.1** (b) **4.2** (c)

Explanations Materials Science

2. Dielectric and Ceramic Materials

2.1 (c)

In an insulating material connected to an a.c. signal, the dielectric constant and atomic polarisation decrease with frequency.



2.3 (a)

In piezoelectric crystals, the mechanical strain may produce an electrostatic charge on the faces of the crystal because the ions in the crystal get displaced and produce dipoles.

3. Magnetic Materials

3.1 (c)

Ferrous ion (Fe^{2+}) has electron configuration
$1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^4$

3d shell | 1 | 1 | 1 | 1 | 0 |

Since number of unpaired electrons = 4
Therefore, magnetic moment
= 4 Bohr magnetron

3.2 (a)

Permanent magnetic materials are those which retain a considerable amount of their magnetic energy after the magnetizing force has been removed, i.e. the materials which are difficult to demagnetize. Therefore for a permanent magnetic material, the residual induction and coercive field should be large.

4. Conductors and Superconductors

4.1 (b)

In superconductor, $B = 0$
or $\mu(H + M) = 0$
$\Rightarrow \quad M = -H$

4.2 (c)

Maximum power handling capacity of a resistor depends on thermal capacity of the resistor.

■■■

6 Electronic Measurements and Instrumentation

1. Basics of Measurement and Error Analysis

1.1 Loading effect is primarily caused by instruments having
(a) high resistance (b) high sensitivity
(c) low sensitivity (d) high range
[ESE-1999]

1.2 The difference between the measured value and the true value is called
(a) gross error (b) relative error
(c) probable error (d) absolute error
[ESE-1999]

1.3 A 300 V full-scale deflection voltmeter has an accuracy of ±2%, when it reads 222 V. The actual voltage
(a) lies between 217.56 V and 226.44 V
(b) lies between 217.4 V and 226.6 V
(c) lies between 216 V and 228 V
(d) is exactly 222 V **[ESE-1999]**

2. Analog Systems for Measurements

2.1 Measurement of an unknown voltage with a dc potentiometer loses its advantage of open-circuit measurement when
(a) the primary circuit battery is changed
(b) standardization has to be done again to compensate for drifts
(c) voltage is larger than the range of the potentiometer
(d) range reduction by a factor of 10 is employed
[ESE-1999]

2.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Former
B. Coil
C. Core
D. Spring

List-II
1. Produces deflecting torque
2. Provides base for the coil
3. Makes the magnetic field radial
4. Provides controlling torque

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	1	2	4	3
(c)	2	1	3	4
(d)	2	1	4	3

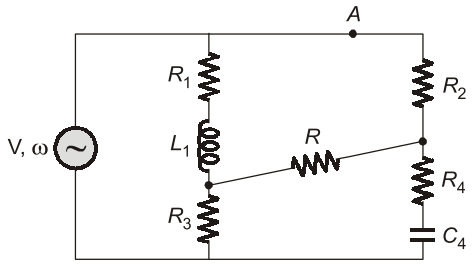
[ESE-1999]

2.3 If the secondary winding of a current transformer opened while the primary winding is carrying current, then
(a) the transformer will burn immediately
(b) there will be weak flux density in the core
(c) there will be a very high induced voltage in the secondary winding
(d) there will be a high current in the secondary winding
[ESE-1999]

2.4 **Assertion (A):** The needle of an indicating instrument attains a position where deflecting and control torques acting on the moving system are equal and opposite.
Reason (R): The oscillations of the needle are suppressed by the damping mechanism.
(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-1999]**

3. Bridge Measurements and Q-meter

3.1 In the circuit shown in the figure, if the current in resistance '*R*' is Nil, then



(a) $\frac{\omega L_1}{R_1} = \frac{1}{\omega C_4 R_4}$

(b) $\frac{\omega L_1}{R_1} = \omega C_4 R_4$

(c) $\tan^{-1}\frac{\omega L_1}{R_1} + \tan^{-1}\omega C_4 R_4 = 0$

(d) $\tan^{-1}\frac{\omega L_1}{R_1} + \tan^{-1}\frac{1}{\omega C_4 R_4} = 0$

[ESE-1999]

3.2 Consider the following operations in respect of a Wheatstone bridge:
(Key "K_b" ; is used for the supply battery and Key "K_g" is used for the galvanometer)

1. Open K_b
2. Close K_g
3. Close K_b
4. Open K_g

The correct sequence of these operations is

(a) 1, 2, 3, 4 (b) 3, 1, 2, 4
(c) 4, 3, 2, 1 (d) 3, 2, 4, 1

[ESE-1999]

3.3 A coil is tuned to resonance at 1 MHz with a resonating capacitance of 72 pF. At 500 kHz, the resonance is obtained with a resonating capacitance value of 360 pF. The self-capacitance of the coil is

(a) 12 pF (b) 24 pF
(c) 36 pF (d) 72 pF

[ESE-1999]

3.4 Match **List-I** (Bridges) with **List-II** (Parameters) and select the correct answer using the codes given below the lists:

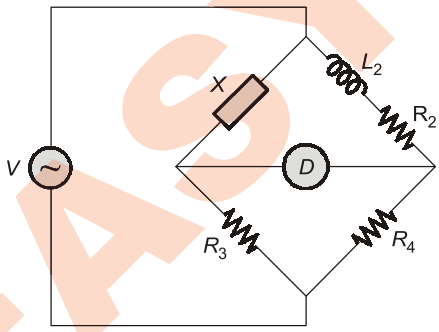
List-I	List-II
A. Anderson bridge	1. Low Resistance
B. Kelvin Bridge	2. Medium Resistance
C. Schering Bridge	3. Inductance
D. Wheatstone Bridge	4. Capacitance

Codes:

	A	B	C	D
(a)	4	2	3	1
(b)	3	2	4	1
(c)	3	1	4	2
(d)	4	1	3	2

[ESE-1999]

3.5 In the balanced bridge shown in the figure, '*X*' should be



(a) a self-inductance having resistance
(b) a capacitance
(c) a non-inductive resistance
(d) an inductance and a capacitance in parallel

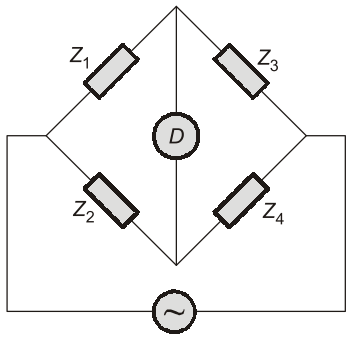
[ESE-1999]

3.6 While using Maxwell bridge, the *Q* factor of a coil is obtained as

(a) $1/\omega CR$ (b) ωCR
(c) $\omega C/R$ (d) $R/\omega C$

[ESE-1999]

3.7 The a.c. bridge shown in the figure is balanced if $Z_1 = 100\ \angle 30°$; $Z_2 = 150\ \angle 0°$; $Z_3 = 250\ \angle -40°$ and Z_4 is equal to

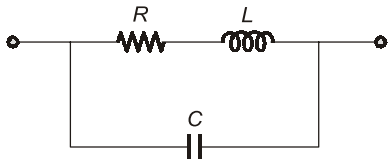


(a) $350\ \angle 70°$ (b) $375\ \angle -70°$
(c) $150\ \angle 0°$ (d) $150\ \angle 20°$

[ESE-1999]

4. Power and Energy Measurement

4.1 The equivalent circuit of a resistor is shown in the given figure. The resistor will be non-inductive if



(a) $R = L/C$ (b) $R = \sqrt{L/C}$

(c) $L = CR^2$ (d) $C = LR^2$ **[ESE-1999]**

5. Cathode Ray Oscilloscope (CRO)

5.1 A dual-trace CRO has
(a) one electron gun
(b) two electron guns
(c) one electron gun and one two-pole switch
(d) two electron guns and one two-pole switch
[ESE-1999]

6. Digital System for Measurement

6.1 A $3\frac{1}{2}$ digit voltmeter having a resolution of 100 mV can be used to measure maximum voltage of
(a) 100 V (b) 200 V
(c) 1000 V (d) 5000 V **[ESE-1999]**

6.2 Consider the following statements:
1. Use of digital computers along with transducers makes data manipulation easier.
2. Digital signals are not dependent on signal amplifiers and so are easy to transmit without distortion and external noise.
3. Increased accuracy in pulse count is possible.
4. There are ergonomic advantages in presenting digital data.

The main advantages of digital transducers include
(a) 1, 2 and 4 (b) 1, 2 and 3
(c) 2, 3, and 4 (d) 1, 2, 3, and 4
[ESE-1999]

6.3 Harmonic distortion analyser
(a) measures the amplitude of each harmonic component
(b) measures the rms value of fundamental frequency component
(c) measures the rms value of all the harmonic components except the fundamental frequency component
(d) displays the rms value of each harmonic component on the screen of a CRO
[ESE-1999]

7. Transducers

7.1 A Hall effect transducer can be used to measure
(a) displacement, temperature and magnetic flux
(b) displacement, position and velocity
(c) position, magnetic flux and pressure
(d) displacement, position and magnetic flux
[ESE-1999]

7.2 Load cell employs
(a) piezoelectric crystal
(b) capacitor
(c) mutual inductance
(d) strain gauges **[ESE-1999]**

7.3 **Assertion (A) :** The capacitive transducer is best suited for measurement of very small pressure differentials under dynamic conditions.
Reason (R) : The capacitance transducer can be excited by both dc and AC voltages.
(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-1999]**

7.4 The device possessing the highest photosensitivity is a
(a) photoconductive cell
(b) photovoltaic cell
(c) photodiode
(d) phototransistor **[ESE-1999]**

8. Data Acquisition Systems and Telemetry Systems

8.1 A 5-channel dc to 60 Hz telemetry system uses PAM and PCM systems. For a good quality data transmission, the minimum sampling rate must be

(a) 300 samples/s (b) 500 samples/s
(c) 1500 samples/s (d) 1250 samples/s

[ESE-1999]

8.2 Which one of the following pairs of Modulation techniques and Telemetry situations and conditions is correctly matched?
(a) Pulse amplitude modulation : Low amplitude signals
(b) Pulse position modulation : For short distances when power is enough
(c) Pulse width modulation : Power to be spent in telemetry is required to be low
(d) Pulse code modulation : Minimisation of interference effects

[ESE-1999]

■■■

Answers Electronic Measurements and Instrumentation

1.1	(c)	1.2	(d)	1.3	(c)	2.1	(c)	2.2	(c)	2.3	(c)	2.4	(b)	3.1	(a)	3.2	(d)		
3.3	(b)	3.4	(c)	3.5	(a)	3.6	(b)	3.7	(b)	4.1	(b, c)	5.1	(c)	6.1	(a)	6.2	(b)		
6.3	(c)	7.1	(d)	7.2	(d)	7.3	(c)	7.4	(b)	8.1	(*)	8.2	(d)						

Explanations Electronic Measurements and Instrumentation

1. Basics of Measurement and Error Analysis

1.1 (c)

Loading effect is primarily caused by instruments having low sensitivity.

1.2 (d)

Absolute error,

$$\delta A = A_m - A_t$$

where, A_m = measured value of quantity
A_t = true value of quantity

1.3 (c)

$$\text{Deflection} = \pm 300 \times \frac{2}{100} = \pm 6 \text{ V}$$

Therefore, the actual voltage = 222 ± 6 V Thus, actual voltage lies between 216 V and 228 V.

3. Bridge Measurements and Q-meter

3.1 (a)

For the bridge to be a balanced, the condition should be

$$(R_1 + j\omega L_1)\left(R_4 + \frac{1}{j\omega C_4}\right) = R_2 R_3$$

On comparing real and imaginary part

$$R_1 R_4 + \frac{L_1}{C_4} = R_2 R_3 \quad \text{...(i)}$$

$$\frac{R_1}{j\omega C_4} + R_4 j\omega L_1 = 0 \quad \text{...(ii)}$$

$$\frac{\omega L_1}{R_1} = \frac{1}{\omega C_4 R_4}$$

3.2 (d)

The steps in the operation of a Wheatstone bridge are as follows:
(i) Close K_b (ii) Close K_g
(iii) Open K_g (iv) Open K_b

3.3 (b)

$$C_D = \frac{C_1 - n^2 C_2}{n^2 - 1}$$

$$n = 2$$

$$C_d = \frac{C_1 - 4C_2}{3} = \frac{360 - 4 \times 72}{3} = 24 \text{ pF}$$

3.4 (c)

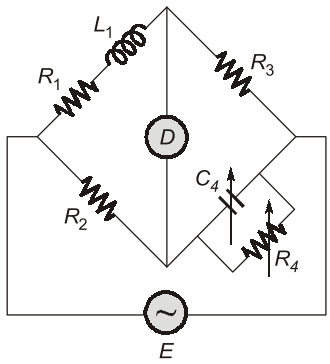
(i) Anderson's bridge method is used to measure the self-inductance in terms of a standard capacitor.

(ii) Kelvin's double bridge method is used for the measurement of low resistance.
(iii) Schering bridge is used to measure the capacitance.

3.5 (a)

The given circuit is Maxwell's inductance bridge.

3.6 (b)



Maxwell's Inductance–Capacitance bridge

At balance, $R_1 = \frac{R_2 R_3}{R_4}$

and $L_1 = C_4 R_2 R_3$

$Q = \frac{\omega L_1}{R_1} = \omega C_4 R_4$

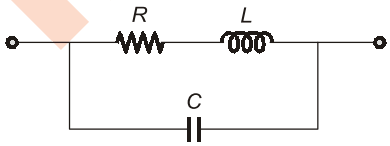
3.7 (b)

$$Z_4 = \frac{Z_2 Z_3}{Z_1}$$

$$= \frac{150\angle 0° \cdot 250\angle -40°}{100\angle 30°} = 375\angle -70°$$

4. Power and Energy Measurement

4.1 (b, c)



Equivalent circuit of resistor

Equivalent impedance,

$$Z = \frac{(1/j\omega C)(R + j\omega L)}{R + j\omega L + (1/j\omega C)}$$

$$= \frac{R + j\omega (L - \omega^2 L^2 C - CR^2)}{1 + \omega^2 C^2 R^2 - 2\omega^2 LC + \omega^4 L^2 C^2}$$

So, the effective reactance,

$$X_{eff} = \frac{\omega\{L(1-\omega^2 LC) - CR^2\}}{1 + \omega^2 C^2 R^2 - 2\omega^2 LC + \omega^4 L^2 C^2}$$

Since X_{eff} is small, we have, $\omega^2 LC << 1$.
So, $\omega^2 LC$ can be neglected.

$$\therefore \quad X_{eff} = \frac{\omega(L - CR^2)}{1 + \omega^2 C(CR^2 - 2L)}$$

If the resistance is non-inductive, then

$$L - CR^2 = 0$$

$$\Rightarrow \quad R = \sqrt{\frac{L}{C}}$$

6. Digital System for Measurement

6.1 (a)

$$\text{Resolution} = \frac{V_{FS}}{10^n}$$

where, V_{FS} = Full scale voltage
So, n = Number of full digital = 3

$$100 \text{ mV} = \frac{V_{FS}}{10^3} \Rightarrow V_{FS} = 100 \text{ V}$$

6.3 (c)

Harmonic distortion analyser is used to measure the total harmonic distortion (THD).

$$\text{THD} = \frac{\left[\Sigma(\text{Harmonics})^2\right]^{1/2}}{\text{Fundamental}}$$

$$\text{or THD} = \sqrt{\left(\frac{E_2}{E_1}\right)^2 + \left(\frac{E_3}{E_1}\right)^2 + \ldots} = \frac{\sqrt{E_2^2 + E_3^2 + \ldots}}{E_1}$$

where, E_n = amplitude of nth harmonic
E_1 = amplitude of fundamental

7. Transducers

7.1 (d)

The principle of Hall effect is that if a specimen (metal or semiconductor) carrying a current I is placed in a transverse magnetic field B, an electric field E is induced in the direction perpendicular to both I and B.
Hall effect transducer can be used to measure
(i) Magnetic flux (ii) Displacement
(iii) Current (iv) Power
(v) Position

7.2 **(d)**

Load cells utilize an elastic member as the primary transducer and strain gauges as secondary transducers.

7.3 **(c)**

The capacitance transducer can be excited only by AC voltages.

8. Data Acquisition Systems and Telemetry Systems

8.1 **(*)**

Minimum sampling rate

$= 2nf_m$

$= 2 \times 5 \times 60$

$= 600$ samples/s

So, in the given options, option (d) is the most suitable.

■■■