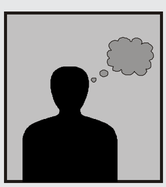
ESE GATE

State Engg. Exams

MADE EASY WORKBOOK 2026



Detailed Explanations of Try Yourself *Questions*

Electronics Engineering

Digital Circuits

MADE EASY PUBLICATIONS

1 Number Systems and Binary Codes

Detailed Explanation of Try Yourself Questions

T1. Sol.

$$\begin{array}{r} 1\ 1\ 1\ 1\ 1 \\ -\ 1\ 0\ 0\ 1\ 1 \\ \hline 1\ 1\ 0\ 0 \\ +\ 1 \\ \hline 1\ 1\ 0\ 1 \end{array}$$

$(1101)_2 = (13)_{10}$

Therefore, the decimal equivalent value = –13.

T2. (d)

Given that,

$$(10)_x \times (10)_x = (100)_x$$
$$x \times x = x^2$$

and

$$(100)_x \times (100)_x = (10000)_x$$
$$x^2 \times x^2 = x^4$$

so, above conditions are valid for all values of x.

T3. (c)

Converting both sides into decimal

$$(2^4 \times 1 + 0 + 2^2 \times w + 2^1 \times 1 + 2^0 \times z) \times 15 = 2^8y + 2^6 \times 1 + 2^4 \times 1 + 2^3 \times 1 + 2^0 \times 1$$
$$(18 + 4w + z) \times 15 = 256y + 64 + 16 + 8 + 1$$
$$270 + 60w + 15z = 256y + 89$$

Only $w = 1$, $z = 1$ and $y = 1$ satisfies.

T4. (a)

$$\begin{array}{r} 9\ 9\ \ \ 9\ 9\ 9 \\ -2\ 5\ .\ 6\ 3\ 9 \\ \hline 7\ 4\ .\ 3\ 6\ 0 \end{array}$$

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2 Logic Gates

Detailed Explanation of Try Yourself Questions

T1. (c)

Bulb is On when both switch S1 and S2 are in same state, either off or on.

S1	S2	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	ON

Above truth table derives EX-NOR operation.

T2. (a)

EXNOR gate on logic in called coincidence logic.

So, $f = AB + A'B'$

T3. (b)

D will be '1' majority of input is 1, so

$$D = A \oplus B \oplus C$$

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3 Combinational Logic Circuits

Detailed Explanation of Try Yourself Questions

T1. (c)

Since the delay is of 1 μsec the output will a square wave with time period of 2 μsec.

So, frequency = 0.5 MHz

T2. (a)

For

A_2	A_1	A_0	S_0 (A_1)	S_1 (A_2)
0	0	0	0	0

MUX is enabled and output is I_0

For

A_2	A_1	A_0	S_0	S_1
0	0	1	0	0

MUX is disable and output is '1'

Similarly, for

A_2	A_1	A_0	S_0	S_1	$\bar{E}$ (A_0)	O/P
0	0	0	0	0	0	I_0
0	0	1	0	0	1	1
0	1	1	0	1	1	1
0	1	0	0	1	0	I_1
1	1	0	1	1	0	I_3
1	1	1	1	1	1	1
1	0	1	1	0	1	1
1	0	0	1	0	0	I_2

T3. (6)

When, T = logic 0, the path followed by the circuit would be,

NOR gate → MUX 1 → MUX 2

⇒ 2 ns → 1.5 ns → 1.5 ns

⇒ 5 ns

When, T = logic 1, the path followed by the circuit would be,

NOR gate → MUX 1 → NOR gate → MUX 2

⇒ 1 ns → 1.5 ns → 2 ns → 1.5 ns

⇒ 6 ns

∴ Maximum propagation delay is 6 ns

T4. (c)

T5. (b)

So, the input to adder is y and 1's complement x since carry input in 1.

So, output is complement of $x + 1$, so output is $y - x$.

T6. (b)

P_1	P_2	a	b	c	d	e	f	g
0	0	1	1	1	1	1	1	0
0	1	1	0	1	1	0	1	1
1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	1	1	1

$a = 1$

$b = \overline{P}_2$ ...1 (NOT)

$c = \overline{P}_1$ ...1 (NOT)

$d = 1 = c + e$

$e = P_1 + \overline{P}_2$ ...1 (OR)

$f = \overline{P}_1 + P_2$ ...1 (OR)

$g = P_1 + P_2$ ... 1 (OR)

⇒ $g = P_1 + P_2$

$d = 1 = c + e$

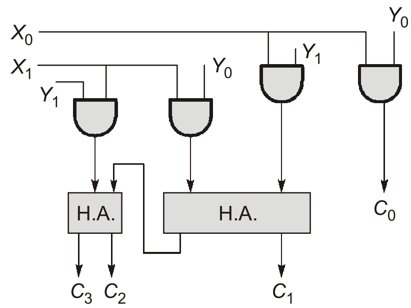
T7. (d)

2 – NOT gates

3 – OR gates

T8. (b)

Two bit binary multiplier



$$\begin{array}{cccc} & & X_1 & X_0 \\ & & Y_1 & Y_0 \\ \hline & & X_1 Y_0 & X_0 Y_0 \\ & X_1 Y_1 & Y_1 X_0 & \\ \hline C_3 & C_2 & C_1 & C_0 \end{array}$$

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4 Sequential Circuits

Detailed Explanation of Try Yourself Questions

T1. (76.92)

Total propagation delay

$= (t_{pd} + t_{set\text{-}up})_{max} = 8\text{ns} + 5\text{ ns} = 13\text{ ns}$

$\therefore$ Frequency of operations

$= \frac{1000}{13}\text{ MHz} = 76.92\text{ MHz}$

T2. (c)

T3. (6)

JK Flip-flop 1 and 2 form a synchronous sequential circuits and they are synchronized with the output of 0^{th} JK Flip-flop.

J_1	K_1	J_2	K_2	Q_2	Q_1	Q_0	
1	1	0	1	0	0	0	T_1
1	1	1	1	0	1	1	T_2
0	1	0	1	1	0	0	T_3
1	1	0	1	0	0	0	

Number of cycles = 3 i.e. equal to 6 clock cycles.

T4. (d)

Trick up/down = $CP \oplus Q$, 1 for up and 0 for down.

CP = (clock pulse)

Q = (O/P)

0 = –ve edge; $Q = 1$

1 = +ve edge; $\bar{Q} = 1$

$= 1 \oplus 1 = 0$ (down counter)

Counting sequence

1	1	1
1	1	0
1	0	1
1	0	0
0	1	1 (preset state) so Mod 5

T5. (b)

T6. Sol.

Clock	Q_A	Q_B	Q_C	Q'_A	Q'_B	Q'_C	$Q_A \oplus Q'_A$	$Q_B \oplus Q'_B$	$Q_C \oplus Q'_C$	Z
0	1	0	0	1	0	0	0	0	0	0
1	0	1	0	1	1	0	1	0	0	1
2	0	0	1	1	1	1	1	1	0	1
3	1	0	0	0	1	1	1	1	1	1
4	0	1	0	0	0	1	0	1	1	1
5	0	0	1	0	0	0	0	0	1	1
6	1	0	0	1	0	0	0	0	0	0

The output Z will again become zero after 6 clock cycles.

T7. (c)

The counter represents a Johnson counter. Thus, total number of states = $2n$. Where $n = 3$.

Therefore the MOD of the counter = $2 \times 3 = 6$

T8. (d)

In a 2^8 Counter the range would be from 0-255.

Hence to go from 10101100 (172) to 00100111 (39), the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255, $255 - 172 = 83$ Clock pulses would be required.

From 255 to 0, again 1 clock pulse would be required.

Then from 0 to 39, 39 clock pulses would be required.

Hence in total $83 + 1 + 39 = 123$ Clock pulses would be required.

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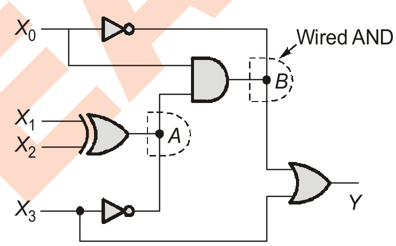
5 Integrated-Circuit Logic Families

Detailed Explanation of Try Yourself Questions

T1. (8)



$$A = (X_1 \oplus X_2)\bar{X}_3$$

$$B = \left[(X_1 \oplus X_2)\bar{X}_3 \; X_0\right] \cdot \bar{X}_0 = 0$$

$$Y = B + X_3 = 0 + X_3 = X_3$$

Out of 16 possible combinations of $X_3\, X_2\, X_1\, X_0$, X_3 will be high for 8 combinations. So, Y will be high for 8 combinations.

T2. (b)

$V_{OH} > V_{IH} > V_{IL} > V_{OL}$.

T3. (b)

It is CMOS gate where 2 PMOS are parallel and in series with 2 NMOS (series combination of NMOS).
It is equivalent to NAND gate.
Series combination of NMOS equivalent to parallel combination of PMOS.

T4. (c)

Truth table:

X	Y	V_0
0	0	1
0	1	0
1	0	0
1	1	0

$$V_0 = \overline{X+Y}$$

T5. (a)

Series combination of n-mos is equivalent to AND and parallel combination is equivalent to OR.

So, $Y = \overline{C.(A+B)} = \overline{C} + \overline{(A+B)} = \overline{C} + \overline{A}.\overline{B}$

T6. (c)

HTL $\rightarrow$ High noise immunity
CMOS $\rightarrow$ Highest fanout
I^2L $\rightarrow$ Lowest of product power and delay
ECL $\rightarrow$ Highest speed of operation

T7. (a)

For TTL logic floating input = 1

$\therefore \quad Y = (AB + 1)' = \overline{AB}.0 = 0$

T8. (a)

ECL is the fastest logic family.

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6 ADC and DAC

Detailed Explanation of Try Yourself Questions

T1. (a)

Sequence of Johnson counter is

Q_2	Q_1	Q_0	D_2	D_1	D_0	V_0
0	0	0	0	0	0	0
1	0	0	1	0	0	4
1	1	0	1	1	0	6
1	1	1	1	1	1	7
0	1	1	0	1	1	3
0	0	1	0	0	1	1
0	0	0	0	0	0	0

T2. (a)

(i) Conversion time is the time taken for a new digital output to appear in response to a change in the input voltage.

(ii) Flash converter is the fastest converter. It uses no clock signal.

(iii)

Type of N-bit ADC	Max. conversion time
• Successive approximation	N clock cycles
• Counter ramp	$2^N - 1$ clock cycles

T3. (c)

Initial stage of the counter = $(111)_2 = (7)_{10}$
So output will be equal to 7 V.
Next state of counter = $(110)_2 = (6)_{10}$
So output should be = 6 V
But output is 3 V that means LSB of counter is connected to MSB of DAC and MSB of counter is connected to LSB of DAC.
Similarly next state of counter = $(101)_2 = (5)_{10}$
Input to DAC = $(101)_2 = (5)_{10}$
So output = 5 V
When counter goes to $(100)_2$ then input to DAC = $(001)_2 = (1)_{10}$
So output = 1 V
So connections are not proper.

T4. (c)

No. of comparators in a flash ADC is equal to $2^n - 1$ where n = no. of bits.
$2^4 - 1 = 15$

T5. (a)

The reference voltage is 5 V.
The number of bits in ADC are 8.

So, the resolution will be = $\dfrac{5}{2^8 - 1} = \dfrac{5}{255}$

The applied input is 3.5 V.
The successive approximation ADC start working from the MSB so.

After one clock:

SAR will toggle it's MSB from $0 \to 1$ so output of *SAR* will be 1000 0000.

After second clock:

SAR will toggle its 7^{th} bit from $0 \to 1$ but 1100 0000 will result in value greater than 3.5 so output of SAR after 2^{nd} clock will be 1000 0000.

After third clock:

SAR will toggle it's 6^{th} bit from $0 \to 1$ and output will be 10100000.

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7 Semiconductor Memories

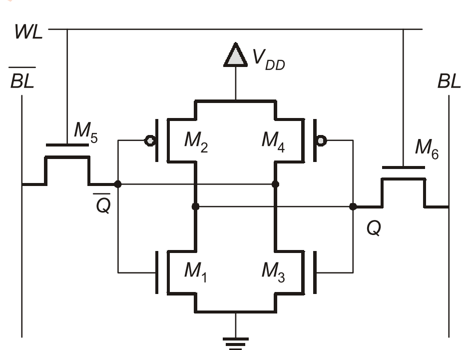
Detailed Explanation of Try Yourself Questions

T1. (b)

				2	4	2	1	
x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0	
0	0	0	0	0	0	0	0	$\rightarrow 0$
0	0	0	1	0	0	0	1	$\rightarrow 1$
0	0	1	0	0	0	1	0	$\rightarrow 2$
0	0	1	1	0	0	1	1	$\rightarrow 3$
0	1	0	0	0	1	0	0	$\rightarrow 4$
0	1	0	1	0	1	0	1	$\rightarrow 5$
0	1	1	0	1	1	0	0	$\rightarrow 6$
0	1	1	1	1	1	0	1	$\rightarrow 7$
1	0	0	0	1	1	1	0	$\rightarrow 8$
1	0	0	1	1	1	1	1	$\rightarrow 9$

$\therefore$ It is 8421BCD to 2421BCD.

T2. (b)



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