ESE

MADE EASY Workbook 2026

Detailed Explanations of Try Yourself *Questions*

Electronics Engineering

Microprocessors

1 Basics of Intel 8085, Intel 8086 and other Microprocessors

T1. **(b)**

In 8085 lower order address bus and data bus are multiplexed to reduce the no. of pins and demultiplexing is done using ALE pin which is when 1 then lower order byte work as address and when 0 work as data.

T2. **(b)**

The first machine cycle of any instruction is opcode fetch cycle.

T3. **(c)**

T4. **(d)**

STA 16-bit address → Store the content of accumulator at 16-bit address.

T5. **(b)**

Ready → 0 ; microprocessor with for I/O
1 ; indicates I/O is ready for communication

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2 8085 Programming

T1. Sol.

(i) *AX* [20] H ⟶ SP ⟶

(ii) *BX* [34] H ⟶ SP ⟶

AX [34] H ⟶ SP ⟵

(iii) 34 H + 34 H = 68 H

CX [20] H ⟶ SP ⟵

Contents of registers.

AX = 68 H
BX = 34 H
CX = 20 H

T2. Sol.

Infinite.

T3. (c)

RST 6.5 and RST 5.5 both are Maskable interrupt.

address location of RST 5.5
$= (8 \times 5.5)_{10} = (44)_{10} = (2C)_{16}$
XTHL ⟶ is a instruction which exchanges top of stack with HL pair.
SID is signal used for serial input data.

T4. (b)

AC ⟹ Auxiliary carry flags status is used only in DAA {DAS}
Decimal adjust after additions {subtraction}
All conditional jumps are short jumps $z = 1$ if data is same when compared.

T5. (a)

SI, DI i.e. source index and destination index registers are used for extra segment (or) alternate date segment.

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3 8085 Microprocessor Interfacing and Applications

T1. Sol.

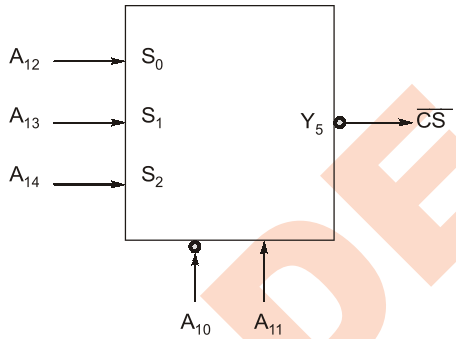
Total Memory of 8085 = 2^{16} bytes

Size of one page = 256 = 2^8 bytes

Number of pages = $\frac{2^{16}}{2^8} = 2^8 = 256$ pages

T2. (d)

1 KB memory is interfaced



A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	$A_9 \ldots A_0$
X	1	0	1	1	0	0.....0
X	1	0	1	1	0	1.....1

If A_{15} =0 $\Rightarrow$ 5800 H to 5 BFFH

If A_{15} =1, $\Rightarrow$ D800H to DBFFH

T3. Sol.

8085 is an 8 bit microprocessor with 8 bit address lines for I/O devices. So, in I/O mapped I/O mode, 8085 can have at most 2^8 = 256 input devices and 256 output devices. Their addresses will lie in the range from 00000000 to 11111111.

T4. (d)

Find whether I/O is I/O mapped I/O or memory mappped I/O.

As per the question $IO/\overline{M}$ signal is connected to $\overline{G_{2A}}$ i.e. $IO/\overline{M} = 0$, hence I/O is allocated address as memory mapped I/O i.e. it has 16-bit address. As it is given in question to access data form I/O, it is an I/P device so instruction must be 'LDA', hence the answer is LDA F8F8H.

By considering the lines A_{15} to A_0, the address F8F8H can be obtained.

T5. Sol.

As per the memory map given

F400H – F7FFH, the decoder input lines values can be found i.e. A_{12}, A_{11} and A_{10}.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
F				4				0				0H			

$\therefore$ A_{12} A_{11} A_0 are 10 1 is 5.

Decoding logic of decoder:

Input			Output
C	B	A	
A_{12}	A_{11}	A_0	
0	0	0	Y_0
0	0	1	Y_1
	⋮		
→ 1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

$\therefore$ Y_5 output is connected to the chip select line of memory.

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