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Important Questions for GATE 2022

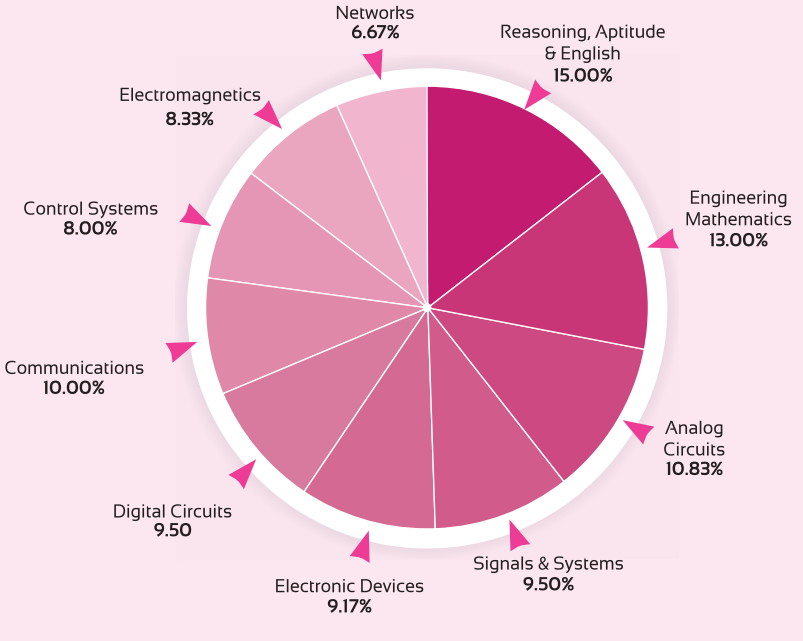
ELECTRONICS ENGINEERING

Day 5 of 8

Q.101 - Q.125 (Out of 200 Questions)

Analog Circuits and Digital Circuits

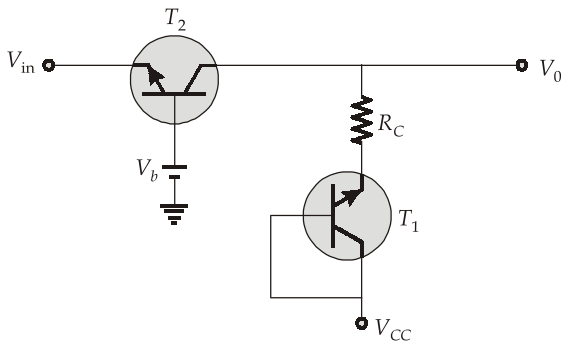
SUBJECT-WISE WEIGHTAGE ANALYSIS OF GATE SYLLABUS



Subject	Average % (last 5 yrs)*
Reasoning, Aptitude & English	15.00%
Engineering Mathematics	13.00%
Analog Circuits	10.83%
Signals & Systems	9.50%
Electronic Devices	9.17%
Digital Circuits	9.50%
Communications	10.00%
Control Systems	8.00%
Electromagnetics	8.33%
Networks	6.67%
Total	**100%**

Analog Circuits and Digital Circuits

Q.101 Consider the circuit shown in the figure below:



In the given figure, biasing conditions are omitted that keeps the transistor in active region. The transistors are biased such that the transconductance of the transistors are given an g_{m1} and g_{m2}, the small signal input resistance is given as $r_{\pi 1}$ and $r_{\pi 2}$ and $r_{01} = r_{02} = \infty$. The value of small signal voltage gain $\frac{V_0}{V_{in}}$ is equal to

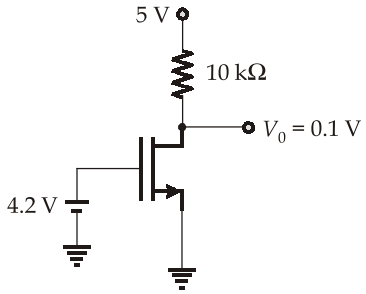
(a) $-g_{m1}\left[R_C + \left(r_{\pi 2} \| g_{m2}\right)\right]$

(b) $+g_{m1}\left[r_{\pi 2} \| 1/g_{m2}\right]$

(c) $+g_{m2}\left[R_C + \left(r_{\pi 1} \| 1/g_{m1}\right)\right]$

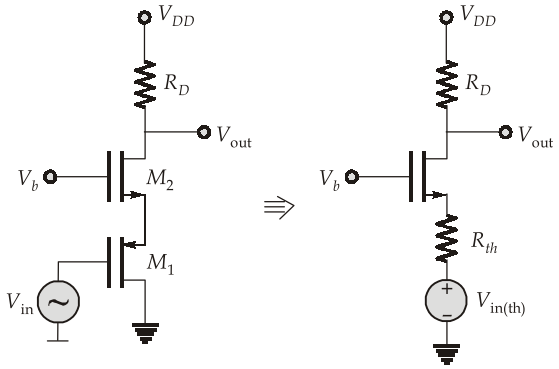
(d) $-g_{m2}\left[r_{\pi 1} \| g_{m1}\right]$

Q.102 Consider the circuit shown in the figure below:



The transistor parameter are given as $V_T = 0.8$ V and $\mu_n C_{ox} = 30\ \mu A/V^2$. The value of $\left(\frac{W}{L}\right)$ for the transistor is equal to _____.

Q.103 Consider the circuit shown in figure



The circuit 2 is equivalent of circuit 1, the M_1 MOSFET of circuit 1 is replaced by its Thevenin equivalent in circuit and thus circuit 1 reduces to a common gate circuit. The value of R_{Th} will be. (Assuming the transconductance of the two MOSFET are g_{m_1} and g_{m_2} and the r_{ds} be r_{o_1} and r_{o_2} respectively)

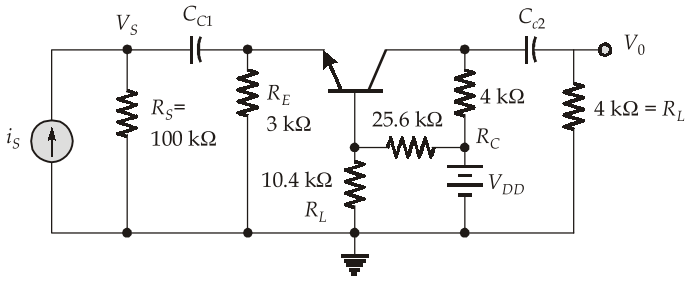
(a) $R_{Th} = r_{o_1} \| \dfrac{1}{g_{m_1}}$

(b) $R_{Th} = r_{o_1} + \dfrac{1}{g_{m_1}}$

(c) $R_{Th} = r_{o_1} + g_{m_1}$

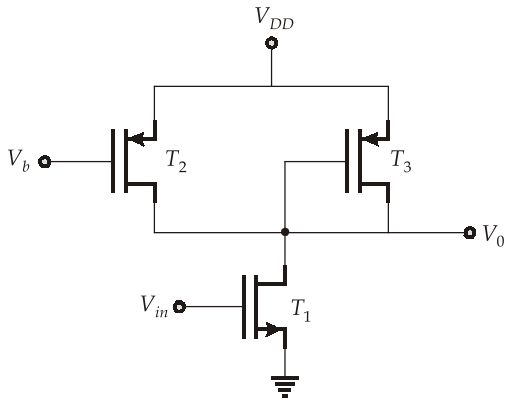
(d) $R_{Th} = r_{o_1} \| g_{m_1}$

Q.104 Consider the circuit shown in the figure below:



Assuming that the transistor is biased in active region with I_{CQ} = 1.46 mA at V_T = 26 mV. The current gain of the transistor is β = 125. Then the value of small signal voltage gain $A_v = V_0/V_s$ for this circuit is equal to _____ V/V.

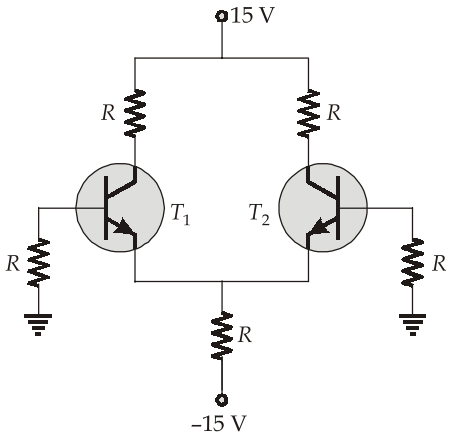
Q.105 Consider the MOS amplifier circuit shown in the figure below:



Assuming all the transistors are operational in saturation region with transconductance g_{m1}, g_{m2} and g_{m3} respectively. There is also the presence of an output small signal intrinsic resistance for the three transistors given as r_{01}, r_{02} and r_{03} respectively. The overall small signal voltage gain for the circuit is equal to

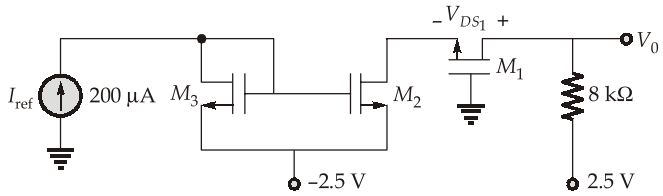
(a) $-g_{m1}(r_{01} \,||\, r_{02} \,||\, r_{03})$
(b) $-g_{m2}(r_{01} \,||\, 1/g_{m2} \,||\, g_{m3})$
(c) $-g_{m1} \cdot g_{m2}(r_{01} \,||\, r_{02} \,||\, r_{03} \,||\, 1/g_{m3})$
(d) $-g_{m1}(r_{01} \,||\, r_{02} \,||\, r_{03} \,||\, 1/g_{m3})$

Q.106 Consider the differential amplifier circuit shown in the figure below:



The two transistors are matched except $\beta_1 = 90$ and $\beta_2 = 110$ with resistance $R = 1$ MΩ. The forward cut in voltage of the two transistors $V_{BE} = 0.7$ V. Then the value of input bias current I_B is equal to _____ nA.

Q.107 Consider the field effect transistor connected in the circuit given below



The threshold voltage for all the transistor is same $V_{TN} = 0.4$ V.

$$\lambda = 0 \quad \text{[for all transistor]}$$

$$\mu_n C_{ox}\left(\frac{W}{2L}\right)_1 = k_{n_1} = 0.25\ \text{mA/V}^2$$

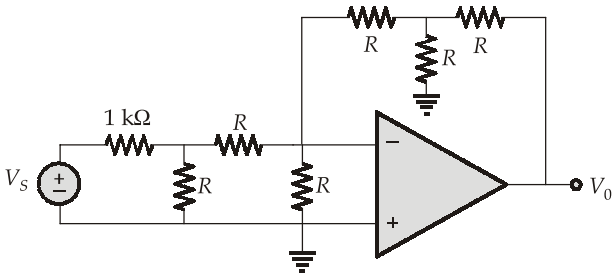
$$\mu_n C_{ox}\left(\frac{W}{2L}\right)_2 = k_{n_2} = \mu_n C_{ox}\left(\frac{W}{2L}\right)_3 = k_{n_3} = 0.15\ \text{mA/V}^2$$

The value of drain to source voltage (V_{DS_1}) of transistor M_1 is

(a) 4.56 V (b) 1.12 V

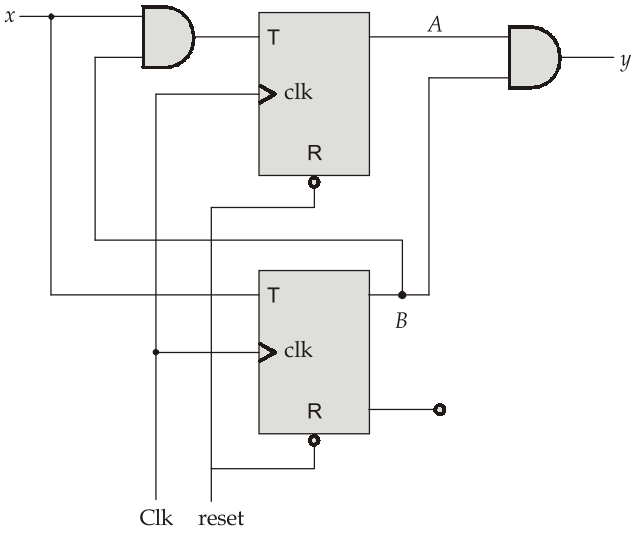
(c) 2.19 V (d) 1.8 V

Q.108 Consider the circuit shown in the figure below:



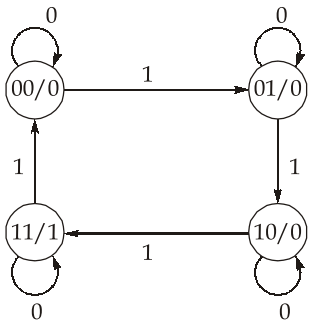
Assume the op-amp to be ideal with resistance $R = 10$ kΩ. Then the value of voltage gain i.e., $\frac{V_0}{V_S}$ is equal to _____ V/V.

Q.109 Consider the sequential circuit with T-flip-flops.

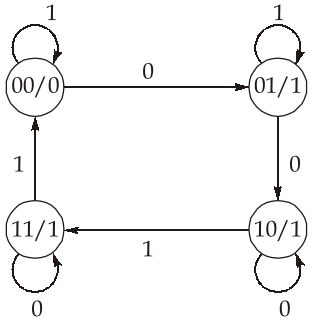


The correct state diagram of the above given circuit is

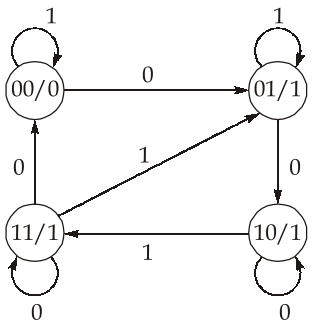
(a)



(b)

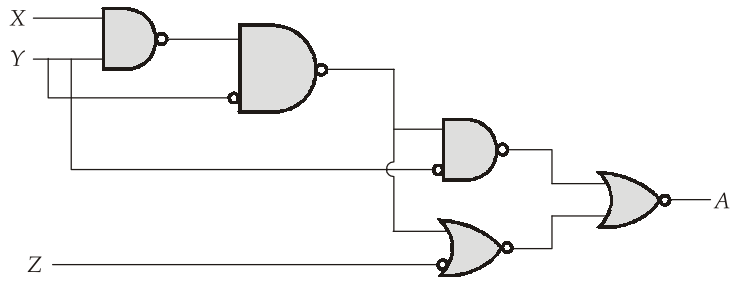


(c)



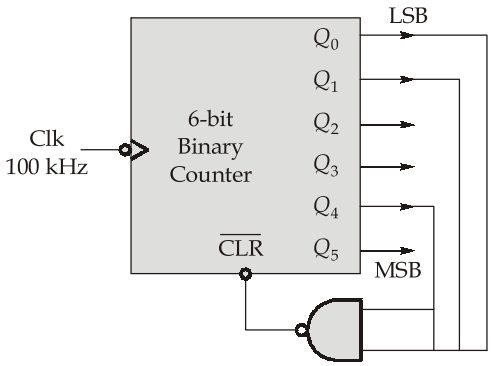
(d) None

Q.110 For the logic circuit shown, the Boolean expression in its simplest form at the output A is



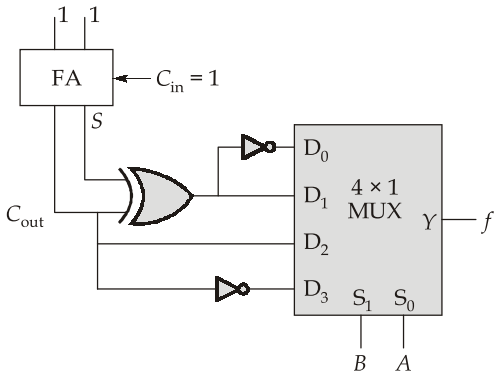
(a) $A = 0$ (b) $A = 1$
(c) $A = Z$ (d) $A = X + Y + Z$

Q.111 A MOD K counter using asynchronous binary up counter with clear input is shown below:



Then the output frequency (f_0) is _____ kHz.

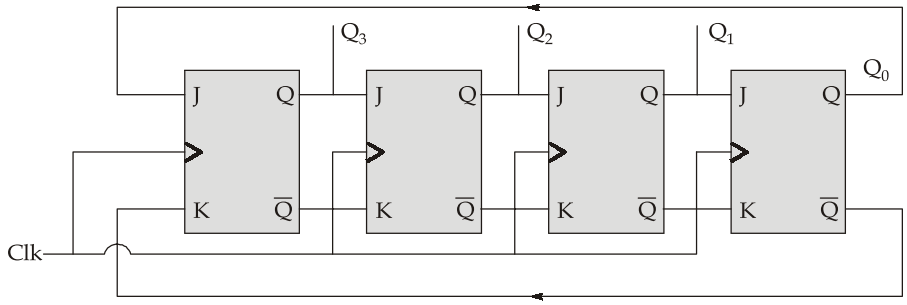
Q.112 Consider the logic circuit shown below:



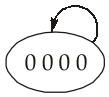
Then the logic expression for output f is

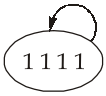
(a) $\overline{A}B$ (b) $A\overline{B}$
(c) $\overline{A}$ (d) $\overline{B}$

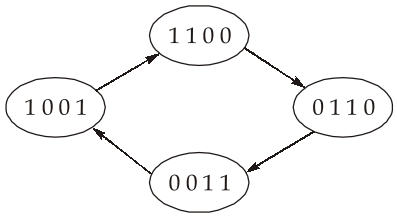
Q.113 Consider a shift register with feedback.

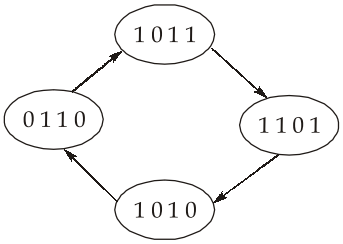


If the serial output of a shift register is connected back to the input $[Q \rightarrow J]$, $\left[\overline{Q} \rightarrow K\right]$. Then which of the following sequence diagram is NOT possible to design with above given circuit.

(a) 

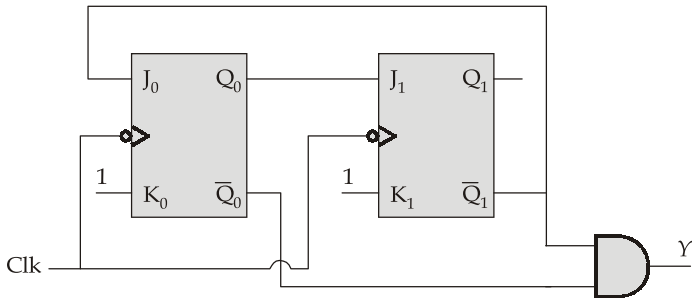
(b) 

(c) 

(d) 

Q.114 Let logic 0 = 0 V and logic 1 = 5 V. Then the output of a 4-bit ladder type digital to analog converter for an input of 1000 is _____. (Using Non-inverting op-Amp)
[Assume all resistors are of equal value]

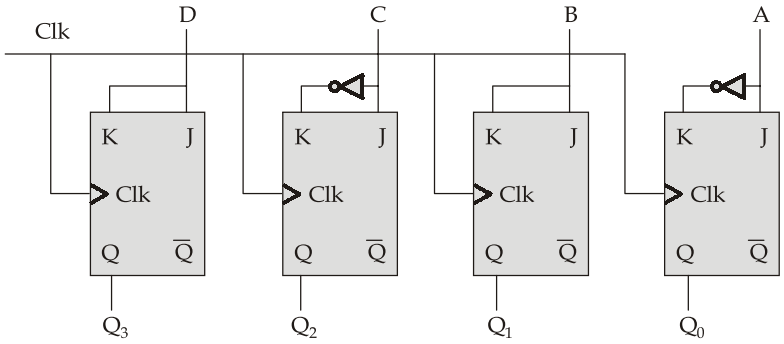
Q.115 For the circuit given below,



The number of clock pulses required for output Y to be at logic high is
[Assume initially all flip flops are clear.]

(a) 1 (b) 2
(c) 3 (d) 4

Q.116 Consider the following logic circuit.

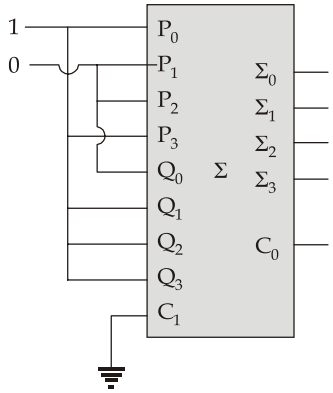


The inputs to the above circuit are fixed at $ABCD$ = 1011 and all flip-flops are cleared initially. After 2nd clock pulse, the output $(Q_3Q_2Q_1Q_0)$ (in decimal) is

(a) 1 (b) 8

(c) 11 (d) 15

Q.117 Consider the digital adder circuit



Then the output of the above adder in the order (C0 Σ3 Σ2 Σ1 Σ0) in decimal is _____.

Q.118 For the k-map shown below, the minimized logical expression in SOP form is

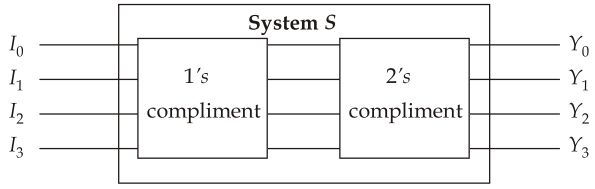
AB \ CD	00	01	11	10
00	1	1		1
01				
11			1	1
10	1		1	1

(a) $\bar{A}\bar{B}\bar{C} + AC + \bar{B}CD + \bar{A}\bar{B}\bar{D}$ (b) $\bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$

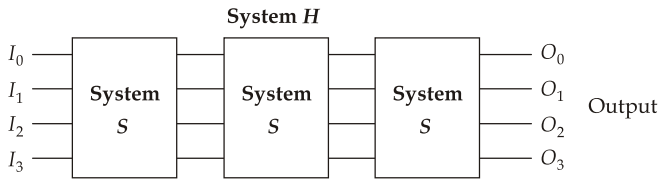
(c) $\bar{A}\bar{B}\bar{C} + AC + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D$ (d) $\bar{A}\bar{B}\bar{C} + AC + \bar{A}\bar{B}\bar{D}$

Q.119 The number of clock pulses needed to change the contents of an 8-bit up-counter from $(10101011)_2$ to $(00111010)_2$ is _____.

Q.120 Consider a **System** *S* as shown in the figure below

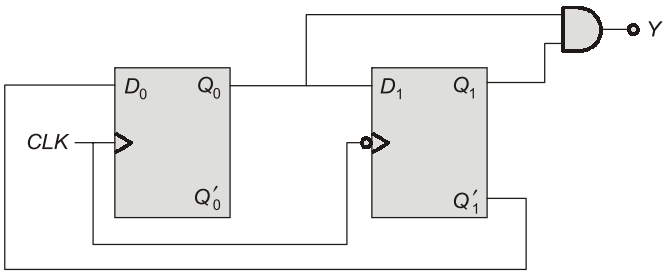


System *S* performs 1's complement of the input and then 2's complement to produce output. A new **System** *H* is designed in which 3 **System** *S* are cascaded



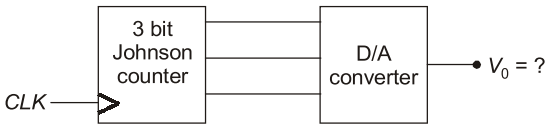
the applied input $(I_3\ I_2\ I_1\ I_0)$ is 1010, then the output $(O_3\ O_2\ O_1\ O_0)$ is _____.

Q.121 The percentage duty cycle of the output *Y*, when the clock frequency is 1 MHz with 50% duty cycle is _____.



Q.122 Assume the Johnson counter is initialized to '000'. The input-output table of digital to analog converter is given below. The output voltage of the D/A converter after applying 3 clock pulses is _____ V.

D/A converter	
Digital Input	**Analog Circuit**
000	0 V
001	1 V
010	2 V
011	3 V
100	4 V
101	5 V
110	6 V
111	7 V



Q.123 Consider the 3 frames main memory initially empty with the following page references

$e, d, h, b, d, e, d, a, e, b, e, d, e, b, g$

The hit ratio using FIFO replacement technique is _____ (in %)

Q.124 Consider a system with 4-way set associative cache of 256 kB. The cache line size is 32 byte. How many bits are used for set offset of cache mapping if main memory addresses are 64 bits long?

(a) 13 bits
(b) 2^{13} bits
(c) 2^{11} bits
(d) 11 bits

Multiple Select Questions (MSQ)

Q.125 Which of the following Boolean identities is/are true?

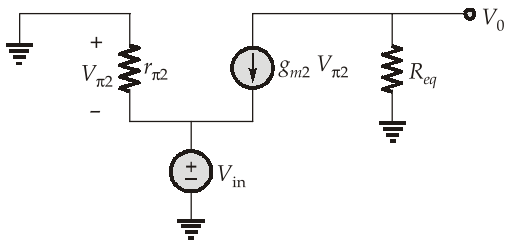
(a) $\overline{A} \oplus B = A \odot B$
(b) $\overline{A} \oplus \overline{B} = A \oplus B$
(c) $(A \oplus B) \oplus AB = A + B$
(d) $(A \oplus B) \oplus AB = \overline{A}B$

■■■■

Detailed Explanations

101. (c)

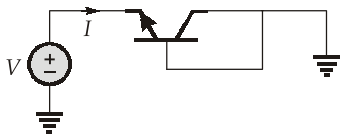
The small signal equivalent circuit for the transistor can be given as



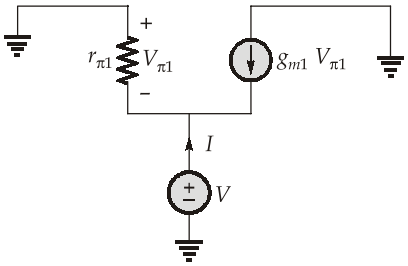
$$\therefore \quad V_0 = -g_{m2}\ V_{\pi 2}\ R_{eq}$$
$$V_0 = -g_{m2}(-V_{in})\ R_{eq}$$
$$V_0 = (g_{m2}\ R_{eq})V_{in}$$

Now, $R_{eq} = R_C + R'$

Where R' is the small signal equivalent resistance of the transistor.



Drawing the small signal equivalent circuit we get



$$\therefore \quad I = -\frac{V_{\pi 1}}{r_{\pi 1}} - g_{m1}V_{\pi 1}$$

$$I = \frac{V}{r_{\pi 1}} + g_{m1}V$$

$$\frac{V}{I} = R' = r_{\pi 1} \| 1/g_{m1}$$

$$\therefore \quad \frac{V_0}{V_{in}} = g_{m2}\left[R_C + (r_{\pi 1} \| 1/g_{m1})\right]$$

102. (48.75) (47.5 to 50)

$$V_{GS} = V_i = 4.2\ \text{V}$$
$$V_{DS} = V_0 = 0.1\ \text{V}$$

Now, $V_{DS} < V_{GS} - V_T$

Thus, the transistor is operating in linear region.

Thus, $$I_D = \frac{\mu_n C_{ox} W}{2L}\left\{2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right\}$$

and $$I_D = \frac{5 - 0.1}{10\,\text{k}\Omega} = \frac{5 - 0.1}{10\,\text{k}\Omega} = 0.49\,\text{mA}$$

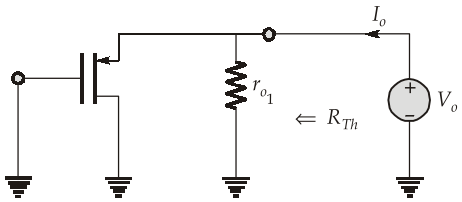
thus, $$0.49 \times 10^{-3} = \frac{30 \times 10^{-6}}{2}\left[\frac{W}{L}\right]\left\{2(4.2 - 0.8)0.1 - (0.1)^2\right\}$$

$$0.49 = \left(\frac{W}{L}\right)10.05 \times 10^{-3}$$

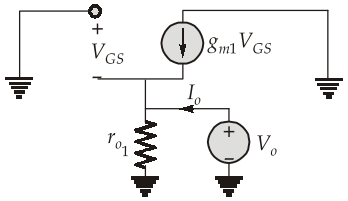
$$\frac{W}{L} = 48.75$$

103. (a)

The above figure can be represented as



For R_{Th} we short circuit V_{in} and apply V_o at the output



$$V_{GS} = -V_o$$

$$\therefore \quad I_o = \frac{V_o}{r_{o_1}} + g_{m_1} V_o$$

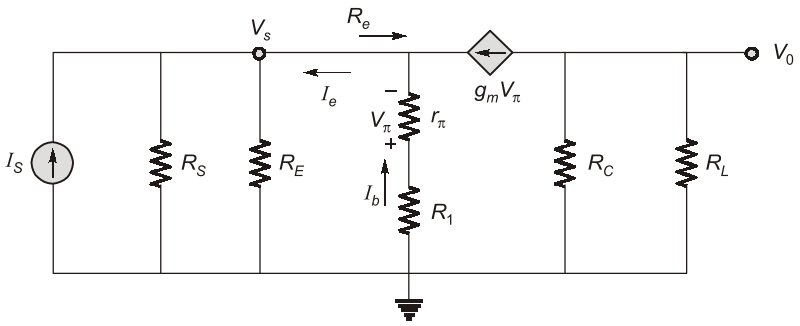
$$\frac{V_o}{I_o} = \left(\frac{1}{r_{o_1}} + g_{m_1}\right)^{-1}$$

$$= r_{o_1} \| \frac{1}{g_{m_1}}$$

104. (26.07) (24 to 28)

$$r_\pi = \frac{(125)(26)}{1.46} = 2.23\,\text{k}\Omega$$

$$g_m = \frac{1.46}{26} = 56.2\,\text{mA/V}$$



$$R_1 = (10.4 \| 25.6)\text{k}\Omega$$
$$R_1 = 7.39\ \text{k}\Omega$$

$$V_\pi = \frac{-r_\pi}{R_1 + r_\pi} V_S$$

$$V_0 = -g_m\, V_\pi\, (R_L \| R_c)$$

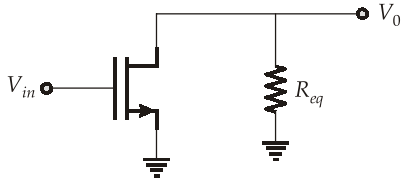
$$\frac{V_0}{V_S} = g_m \times \frac{r_\pi}{R_1 + r_\pi} \times \left(R_L \| R_C\right)$$

$$\frac{V_0}{V_S} = 26.04\ \text{V/V}$$

105. (d)

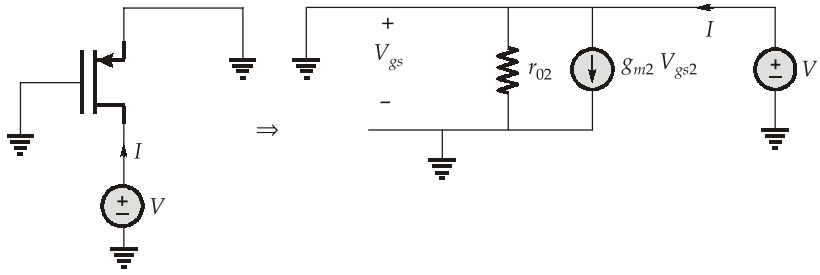
The overall gain of the transistor is given as

$$A_V = -g_{m1}\, R_{eq}$$



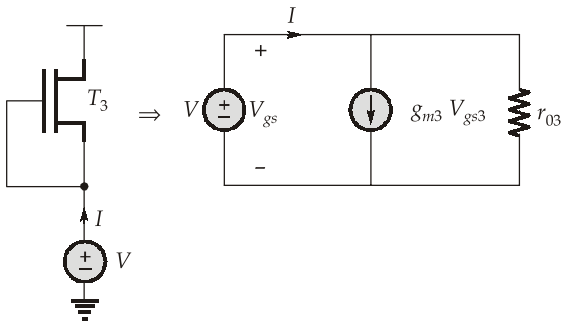
now, R_{eq} will be equal to the parallel combination of the equivalent resistance seen at the output terminal.

1. Equivalent output resistance of transistor T_1 is equal to r_{01}
2. Equivalent resistance due to transistor T_2 can be calculated as



thus $$\frac{V}{I} = r_{02}$$

3. Equivalent resistance due to transistor T_3



$$\therefore \quad I = \frac{V}{r_{03}} + g_{m3}V$$

$$\text{or} \quad \frac{V}{I} = \left(r_{03} \| 1/g_{m3}\right)$$

$$\therefore \quad R_{eq} = r_{01} \| r_{02} \| r_{03} \| \frac{1}{g_{m3}}$$

$$\therefore \quad \frac{V_0}{V_i} = -g_{m1}\left(r_{01} \| r_{02} \| r_{03} \| 1/g_{m3}\right)$$

106. 70.622 (69 to 72)

Input bias current

$$I_B = \frac{I_{B_1} + I_{B2}}{2}$$

Now, applying KVL in base emitter loop we get

$-I_{B1} \times 1 \times 10^6 - V_{BE} - (I_{E1} + I_{E2}) \times 1 \times 10^6 + 15 = 0$

Now, $I_{E1} = 91\, I_{B1}$

and $I_{E2} = 111\, I_{B2}$

Thus, $-I_{B1} \times 10^6 - V_{BE} - (91 I_{B1} + 111\, I_{B2}) \times 10^6 = -15$

$-92 \times 10^6\, I_{B1} - 111 \times 10^6\, I_{B2} = -15 + V_{BE}$ ...(1)

and $-I_{B2} \times 10^6 - V_{BE} - (I_{E1} + I_{E2}) \times 10^6 + 15 = 0$

$-91 \times 10^6\, I_{B1} - 112 \times 10^6\, I_{B2} = -15 + V_{BE}$ ...(2)

Subtracting equation (1) from equation (2) we get

$$I_{B1} = I_{B2}$$

Dividing equation (1) by 111×10^6 and equation (2) by 112×10^6 we get,

$$-0.8288\, I_{B1} - I_{B2} = 9.009 \times 10^{-9}(-15 + V_{BE}) \quad \text{...(3)}$$

$$-0.8125\, I_{B1} - I_{B2} = 8.9285 \times 10^{-9}(-15 + V_{BE}) \quad \text{...(4)}$$

substracting (4) from (3) we get

$$-0.0163 I_{B1} = 9.009 \times 10^{-9}(-15 + V_{BE}) - 8.9285 \times 10^{-9}(-15 + V_{BE})$$

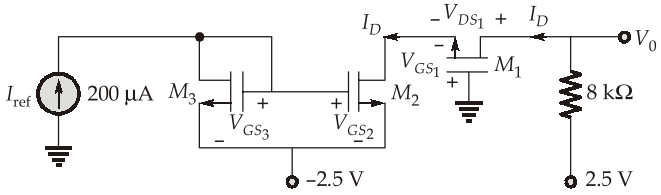
Now $V_{BE} = 0.7$

$$\therefore \quad -0.0163\, I_{B1} = -1.1511 \times 10^{-9}$$

$$I_{B1} = 70.622 \text{ nA}$$

$$\therefore \quad I_B = \frac{I_{B1} + I_{B2}}{2} = 70.622 \text{ nA}$$

107. **(c)**



$$I_D = I_{ref} = 200\ \mu A \qquad \text{[by current mirror action]}$$

$$I_{D_3} = k_{n_3}(V_{GS_3} - V_{TN})^2$$

$$V_{GS_3} = \sqrt{\frac{I_{DS}}{k_{n_3}}} + V_{TN} = \sqrt{\frac{0.2}{0.15}} + 0.4 = 1.555\ V$$

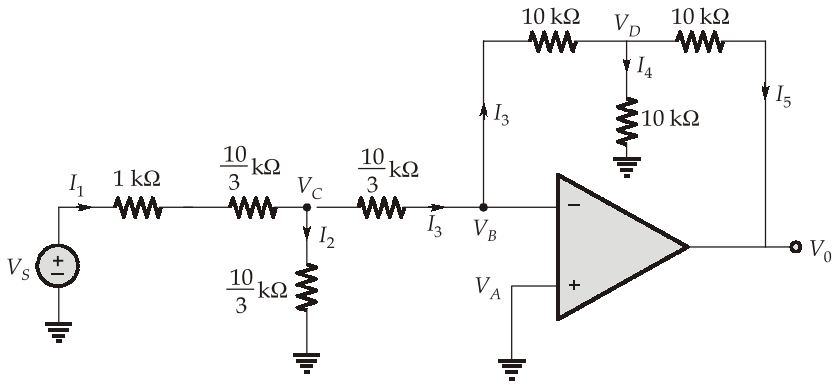
$$V_{GS_3} = V_{GS_2} = 1.555\ V$$

$$V_{GS_1} = \sqrt{\frac{I_D}{k_{n_1}}} + V_{TN} = \sqrt{\frac{0.2}{0.25}} + 0.4 = 1.29\ V$$

$$V_{DS_1} = V^+ - I_D R_D - (V_{GS_1})$$
$$= 2.5 - 0.2 \times 8 - (-1.29)$$
$$V_{DS_1} = 2.19\ V$$

108. **(–2.5) (–2.7 to –2.3)**

Applying star to delta conversion we get,



now, $V_A = V_B = 0$ V due to virtual ground.

$$I_1 = \frac{V_S - V_C}{\left[1 + \frac{10}{3}\right] \times 10^3} = \frac{V_S - V_C}{4.33 \times 10^3}$$

$$I_2 = \frac{V_C}{\frac{10}{3} \times 10^3} \qquad \text{and} \qquad I_3 = \frac{V_C - V_B}{\frac{10}{3} \times 10^3} = \frac{V_C}{\frac{10}{3} \times 10^3}$$

Applying KCL at node C, we get,

$$\frac{V_S - V_C}{\frac{13}{3} \times 10^3} - \frac{V_C}{\frac{10}{3} \times 10^3} - \frac{V_C}{\frac{10}{3} \times 10^3} = 0$$

$$\frac{V_S}{\frac{13}{3}} = \frac{V_C}{10/3} + \frac{V_C}{10/3} + \frac{V_C}{13/3}$$

$$\therefore \quad V_S = 3.6\ V_C$$

and $$I_3 = \frac{V_B - V_D}{10\times10^3} = -\frac{V_D}{10\times10^3}$$

$$I_4 = \frac{V_D}{10\times10^3}$$

and $$I_5 = \frac{V_D - V_0}{10\times10^3}$$

Now, applying KCL at node 'D' we get

$$\frac{-V_D}{10\times10^3} - \frac{V_D}{10\times10^3} - \frac{V_D - V_0}{10\times10^3} = 0$$

$$\Rightarrow \quad V_0 = 3V_D$$

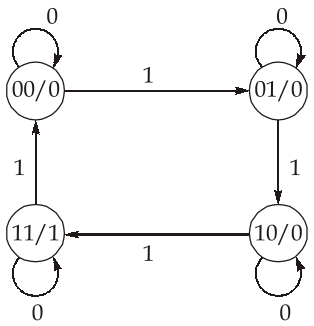
thus, $$\frac{V_C}{\frac{10}{3}\times10^3} = \frac{-V_D}{10\times10^3}$$

$$\frac{V_S}{3.6\times\frac{10}{3}\times10^3} = -\frac{V_0}{3\times10\times10^3}$$

$$\frac{V_0}{V_S} = -2.5\ \text{V/V}$$

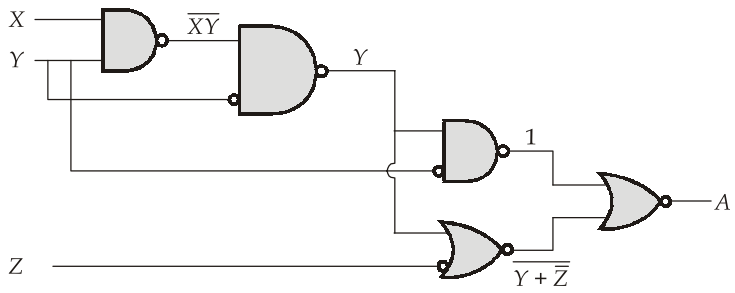
109. (a)

Present state		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	0	0



110. **(a)**

Given,



$$A = \overline{1+\bar{Y}Z}$$

$$= \bar{1}\cdot\overline{\bar{Y}Z}$$

$$A = 0$$

111. **5.26 (5.1 to 5.4)**

When input to NAND is all one then the given 6-bit binary counter is cleared i.e., $Q_4\,Q_1\,Q_0$ is to be 111

$\therefore$

Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	1	0	0	1	1	$\rightarrow (19)_{10}$

i.e., 0 – 18

$\therefore$ The given counter is MOD-19 counter

$\therefore$ Output frequency $f_0 = \dfrac{100\text{ K}}{19} = 5.26\text{ kHz}$

112. **(c)**

For full adder with given input

Sum, $S = 1$ and $C_{out} = 1$

$\therefore$ $D_0 = 1;\ D_1 = 0;\ D_2 = 1,\ D_3 = 0$

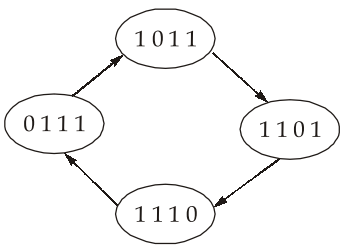
$$f = \bar{A}\bar{B}(1) + B\bar{A}(1)$$

$$= \bar{A}$$

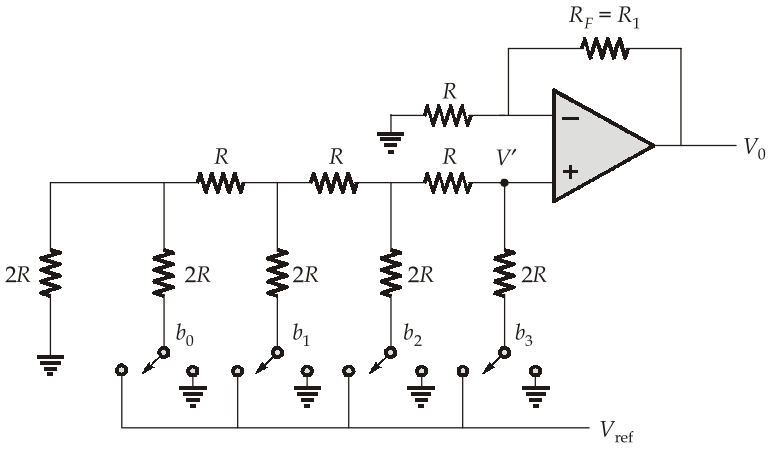
113. **(d)**

Clk	Q_3	Q_2	Q_1	Q_0
0	1	0	1	1
1	1	1	0	1
2	1	1	1	0
3	0	1	1	1
4	1	0	1	1

The correct sequence



114. **5 (4.8 to 5.2)**



Given, $b_3\, b_2\, b_1\, b_0 = 1000$

$$\therefore \quad \frac{V'}{2R} + \frac{V'-5}{2R} = 0$$

$$V' = 2.5$$

$$V_0 = \left[1 + \frac{R_F}{R}\right] V'$$

$$= [1 + 1]2.5 = 5 \text{ V}$$

115. **(c)**

	Clk	Q_0	Q_1	Y
(initially)	0	0	0	1
	1	1	0	0
	2	0	1	0
	3	0	0	1

116. **(a)**

Since Q_2 and Q_0 are output of D-FF.

Q_3 and Q_1 are output of T-FF.

Clk	A	B	C	D	Q_3	Q_2	Q_1	Q_0
Initial	1	0	1	1	0	0	0	0
1	1	0	1	1	1	0	1	1
2	1	0	1	1	0	0	0	1

So, after 2nd clock pulse, $(Q_3Q_2Q_1Q_0) = (0001)_2 = (1)_{10}$

117. **(23)**

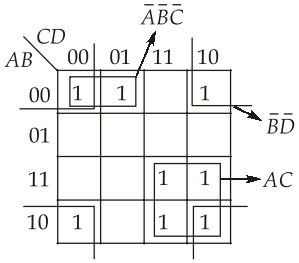
For the given adder,

$$\Sigma 0 = P_0 + Q_0 = 1 + 0 = 1$$
$$\Sigma 1 = P_1 + Q_1 = 0 + 1 = 1$$
$$\Sigma 2 = P_2 + Q_2 = 0 + 1 = 1$$
$$\Sigma 3 = P_3 + Q_3 = 1 + 1 = 0 \text{ (carry } C_0 = 1)$$

$\therefore$ $(C0, \Sigma 3, \Sigma 2, \Sigma 1, \Sigma 0) = (10111)_2 = (23)_{10}$

118. **(b)**

The k-map can be grouped as



$$F = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$$

119. **(143)**

Number of states for 8-bit up-counter = $2^8 = 255$

thus the counter ranges from –0 to 255

Hence, to go from $(10101011)_2 = (171)_{10}$ to $(00111010)_2 = (58)_{10}$

The counter has to go initially from 171 to 255 and then from 0 to 58.

Hence,

from 171 to 255 = 255 – 171 = 84 clock pulse required

from 255 to 0 = 1 clock pulse required

and from 0 to 58 = 58 clock pulse required

$\therefore$ The total number of clock pulse required is

= 84 + 1 + 58

= 143

Alternatively

Total number of clock pulse required = $[2^n - (\text{present state})_{10}] + (\text{desired state})_{10}$

= $(2^8 - 171) + 58 = 143$

120. **(1101)**

Let a number N is given to the system

output after 1's complement = 15 – N

output after 2's complement = 16 – 15 + N = N + 1

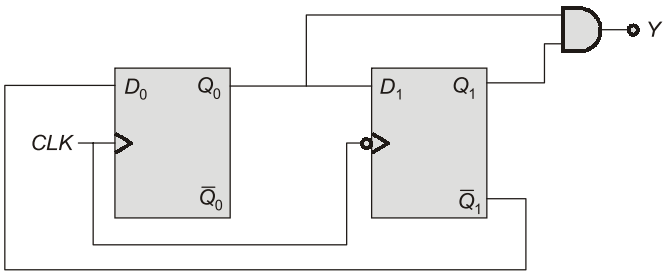
3 such systems are connected in cascade.

so final output = Input + $(3)_{10}$ = 1010 + 0011

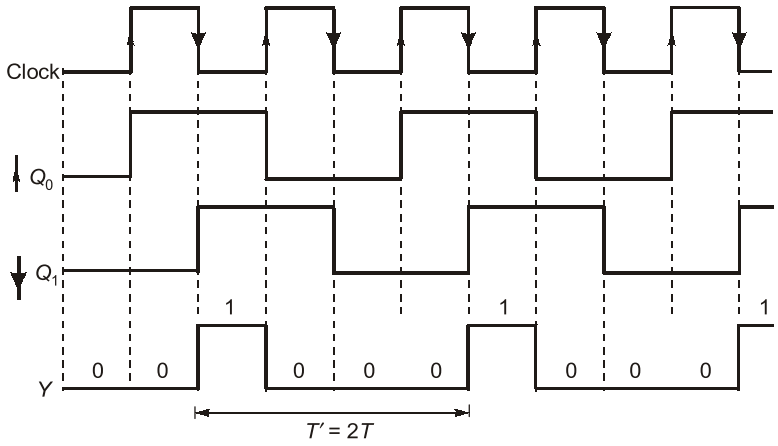
= 1101

121. **(25)**

Assume the output of both the flip-flops is 0 initially.



Waveforms :



$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON}+T_{OFF}} \times 100\% = \frac{1}{1+3} \times 100\%$$

$$= \frac{1}{4} \times 100\% = 25\%$$

122. (7)

3-bit Johnson counter

CLK	Present state	Next state
0	0 0 0	0 0 0
1	0 0 0	1 0 0
2	1 0 0	1 1 0
3	1 1 0	1 1 1
4	1 1 1	0 1 1

Hence output of Johnson counter after 3 clock pulses = 111

Therefore, output of D/A converter = 7 V

123. (26.67) (26.00 to 27.00)

	e	*d*	*h*	*b*	*d*	*e*	*d*	*a*	*e*	*b*	*e*	*d*	*e*	*b*	*g*
0	*e*	*e*	*e*	*b*	*b*	*b*	*b*	*a*	*a*	*a*	*a*	*d*	*d*	*d*	*d*
1		*d*	*d*	*d*	*d*	*e*	*e*	*e*	*e*	*b*	*b*	*b*	*b*	*b*	*g*
2			*h*	*h*	*h*	*h*	*d*	*d*	*d*	*d*	*e*	*e*	*e*	*e*	*e*
					*				*				*	*	

Page hits = 4

Total pages = 15

$$\text{Hit ratio} = \frac{\text{Page hits}}{\text{Total pages}} = \frac{4}{15} = 0.2667$$

% Hit ratio = 26.67%

124. **(d)**

$$\text{Cache memory size} = 256 \times 2^{10} \text{ byte} = 2^{18} \text{ byte}$$

$$\text{Block (line) size} = 32 \text{ byte} = 2^5 \text{ byte}$$

$$\text{Number of lines n cache memory } [N] = \frac{2^{18}}{2^5} = 2^{13}$$

$$\text{Number of set} = \frac{\text{Number of lines in cache memory}}{P\text{-way}} = \frac{2^{13}}{2^2} = 2^{11}$$

$$\therefore \quad \text{Set offset} = \log_2[\#\text{set}] = \log_2[2^{11}] = 11 \text{ bits}$$

125. **(a, b, c)**

(i) $\overline{A} \oplus B = \overline{(\overline{A})}B + \overline{A}\overline{B}$

$= AB + \overline{A}\overline{B} = A \odot B$

(ii) $\overline{A} \oplus \overline{B} = \overline{\overline{A}}\,\overline{B} + \overline{A}\overline{\overline{B}}$

$= A\overline{B} + \overline{A}B = A \oplus B$

(iii) $(A \oplus B) \oplus AB = (A \oplus B) \cdot \overline{AB} + \overline{(A \oplus B)} \cdot AB$

$= (\overline{A}B + A\overline{B})(\overline{A} + \overline{B}) + (\overline{A}\overline{B} + AB) \cdot AB$

$= \overline{A}B + A\overline{B} + AB$

$= A + \overline{A}B$

$= A + B$

■■■■