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Computer Organization

Contents

Sl. Topic	Page No.
1. Basics of Computer Design	2
2. CPU Design	22
3. Instruction Pipelining	34
4. Memory Hierarchy Design	52
5. Input-Output and Secondary Storage	75
6. Data Representation	87



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Instruction Pipelining

- Q.1** Pipelining improves CPU performance due to
- (a) reduced memory access time
 - (b) increased clock speed
 - (c) the introduction of parallelism
 - (d) additional functional units
- Q.2** An instruction cycle refers to
- (a) fetching an instruction
 - (b) clock speed
 - (c) fetching, decoding and executing an instruction
 - (d) executing an instruction
- Q.3** The performance of a pipelined processor suffers if
- (a) the pipeline stages have different delays
 - (b) consecutive instructions are dependent on each other
 - (c) the pipeline stages share hardware resources
 - (d) all of the above
- Q.4** What will be the efficiency (in percentage) of the pipeline if 5 stage pipelined with the respective delay of 20, 30, 40, 50, 60?
- Q.5** An instruction cycle refers to
- (a) Fetching an instruction
 - (b) Clock speed
 - (c) Fetching, decoding and executing an instruction
 - (d) Executing an instruction
- Q.6** A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be
- (a) 120.4 ms (b) 160.5 ms
 - (c) 165.5 ms (d) 590.0 ms
- Q.7** Pipelining is an implementation technique where multiple instructions are overlapped in execution. What among the given is the function of the pipeline.
- (a) Increase the length of machine cycle
 - (b) Decrease the individual instruction execution time.
 - (c) Increase the instruction throughput
 - (d) None of these
- Q.8** Assume the individual stages of the data path have the following latencies.
- Instruction decode (ID): 8ns
Execution (EX) : 6 ns
Memory (MEM) : 9 ns
Write back (Wb) : 5 ns
- Find the clock cycle time (in ns) in a non-pipelined (single cycle) processor.
- (a) 40 (b) 60
 - (c) 35 (d) 45
- Q.9** Pipelining is an implementation technique where multiple instructions are overlapped in execution. What among the given is the function of the pipeline.
- (a) Increase the length of machine cycle.
 - (b) Decrease the individual instruction execution time.
 - (c) Increase the instruction throughput
 - (d) None of these
- Q.10** The performance of a pipelined processor suffers if
- (a) the pipeline stages have different delays
 - (b) consecutive instructions are dependent on each other
 - (c) the pipeline stages share hardware resources
 - (d) All of the above

Q.11 Assume the individual stages of the data path have the following latencies.

Instruction Fetch (IF) : 10 ns
Instruction Decode (ID) : 8 ns
Execution (EX) : 6 ns
Memory (MEM) : 9 ns
Write Back (WB) : 5 ns

Find the clock cycle time in a non-pipelined (single cycle) processor?

- (a) 10 ns (b) 18 ns
(c) 28 ns (d) 38 ns

Q.12 Consider the following instructions.

$I_1: R_1 = 100$
 $I_2: R_1 = R_2 + R_4$
 $I_3: R_2 = R_4 + 25$
 $I_4: R_4 = R_1 + R_3$
 $I_5: R_1 = R_1 + 30$

Calculate sum of (WAR, RAW and WAW) dependencies the above instructions.

- (a) 10 (b) 12
(c) 7 (d) 8

Q.13 Consider a pipelined system with four stages: IF, ID, EX, WB. Following chart shows the clock cycles required by each instruction to complete each stage.

Instructions	Instruction Fetch (IF)	Instruction Decode (ID)	Instruction Execute (EX)	Write Back (WB)
I_0	1	1	2	1
I_1	2	2	3	1
I_2	2	2	2	2
I_3	2	1	1	1
I_4	3	2	1	2

How many clock cycles are required to complete the above instructions?

- (a) 16 (b) 9
(c) 14 (d) 13

Q.14 Consider the unpipelined machine with 10 ns clock cycles. It uses four cycles for ALU operations and branches, whereas five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, 40% respectively. Suppose that due to clock skew and setup, pipelining the machine adds 1 ns overhead to the clock. How much speed up in the instruction execution rate will we gain from a pipeline?

- (a) 5 times (b) 8 times
(c) 4 times (d) 4.5 times

Q.15 Consider a hypothetical processor operating on 500 MHz frequency which uses different operand accessing mode described below:

Operand Fetching Mode	Frequency (%)
Indirect addressing mode	25
Direct addressing mode	30
Register addressing mode	20
Register indirect addressing mode	15
Indexed addressing mode	10

Consider the following data regarding different operations performed:

Operation	No. of cycle needed
Memory Reference (MR)	8
ALU operation (ALU)	4
Register Reference (RR)	0

The average operand fetch rate of CPU is _____ MIPS.

- (a) 40.8 (b) 56.8
(c) 60.8 (d) 58.7

Q.16 Consider the following sequence of instructions

1. LOAD F4, 16(R2)
2. LOAD F6, 48(R2)
3. MUL F10, F4, F8
4. Add F8, F10, F6
5. STORE F8, O(R3)

The number of stalls cycles during the execution of these instructions on the regular 5 stage pipelined processor is _____ (Assume that the pipeline stages are IF, ID, EX, MEM, WB).

Q.17 We have two designs D_1 and D_2 for a synchronous pipeline processor. D_1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D_2 has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design D_2 over design D_1 for executing 100 instructions?

- (a) 214 nsec (b) 202 nsec
(c) 86 nsec (d) 200 nsec

Answers Instruction Pipelining

1. (c) 2. (c) 3. (d) 4. (67) 5. (c) 6. (c) 7. (c) 8. (a) 9. (c)
 10. (d) 11. (d) 12. (c) 13. (a) 14. (c) 15. (b) 16. (5) 17. (b) 18. (78)
 19. (d) 20. (28) 21. (c) 23. (d) 24. (219) 25. (c) 26. (a) 27. (d) 28. (d)
 29. (b) 30. (a) 31. (b) 32. (c) 33. (64) 34. (c) 35. (a) 36. (c) 37. (a)
 38. (d) 39. (a) 40. (d) 41. (c) 42. (c) 43. (b) 45. (b) 46. (c) 47. (c)
 48. (b) 50. (b) 52. (22.2) 54. (4) 55. (b) 56. (b) 57. (50) 58. (6.75) 60. (a)
 61. (b)

Explanations Instruction Pipelining

1. (c)

In pipelining, a number of functional units are employed in sequence to perform a single computation.

3. (d)

The performance of a pipelined processor depends upon delays of different stage and its hardware resources also it depends upon consecutive instructions format.

4. (67)

Pipeline with 5 stages

$$K = 5$$

$$\text{Max delay} = 60$$

$$\eta(\text{efficiency}) = \frac{5}{K} = \frac{200}{60}$$

$$\eta = 3.33$$

$$\eta = \frac{5}{K} = \frac{2.83}{5} = 0.67$$

67% efficiency

5. (c)

An instruction cycle is the basic operational process of a computer. It is the process by which a computer retrieves a program instruction from its memory, determines what actions the instruction dictates and carries out those actions. Also called as fetch, decode-execute cycle.

6. (c)

K stage pipeline can process n tasks in T_K time

$$T_K = [K + (n - 1)] t$$

When $\tau = \tau_m + d$ where τ_m is the maximum stage delay so $\max(150, 120, 160, 140) = 160$

$$\tau = 160 + 5 = 165 \text{ ns}$$

$$\tau = 165 \times 10^{-3} \text{ ms}$$

$$K = 4, n = 1000$$

$$T = [4 + (1000 - 1)]\tau$$

$$= 1003 \times 165 \times 10^{-3} = 165.5 \text{ ms}$$

7. (c)

The throughput of the instruction pipeline is determined by how often an instruction exists the pipeline or the number of instructions that can be executed in a unit of time and this is the function of pipeline.

8. (a)

$$\begin{aligned} \text{Clock cycle time} &= 12 + 8 + 6 + 9 + 5 \\ &= 40 \text{ ns (nonpipelined)} \end{aligned}$$

9. (c)

Function of pipelining is to make cycle per instruction = 1 first, for that instructions are overlapped and hence the instruction throughput is increased.

10. (d)

If the pipeline stages have different delay, then the maximum of all the delays is taken for every stage. If consecutive instruction are dependent on each other or if the pipeline stages share hardware resources, it will create stalls.

Hence all the condition will lead to an impact on the performance of pipelined processor.

11. (d)

$10 + 8 + 6 + 9 + 5 = 38$ ns in non-pipelined.

12. (c)

RAW	WAR	WAW
In-Out	Out-In $I_3 \rightarrow I_2$ $I_4 \rightarrow I_2$ $I_4 \rightarrow I_3$ $I_5 \rightarrow I_4$	Out-Out $I_2 \rightarrow I_1$ $I_5 \rightarrow I_1$ $I_5 \rightarrow I_2$
= 0	= 4	= 3

Sum = $(0 + 4 + 3) = 7$

13. (a)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
I_0	IF	ID	EX	EX	WB											
I_1		IF	IF	ID	ID	EX	EX	EX	WB							
I_2				IF	IF	ID	ID		EX	EX	WB	WB				
I_3						IF	IF		ID		EX		WB			
I_4									IF	IF	IF	ID	ID	EX	WB	WB

It requires 16 clock cycles.

14. (c)

Operation	Frequency	Clock cycles
ALU	40%	4
Branch	20%	4
Memory	40%	5

Total clock cycle

$$= 0.40 \times 4 + 0.20 \times 4 + 0.40 \times 5$$

$$= 16.0 + 0.8 + 2 = 4.4 \text{ clock cycle}$$

Under non pipeline time = $4.4 \times (10) = 44$

Under pipeline time = $10 + \text{overhead} = 10 + 1 = 11$

$$\text{So, speedup} = \frac{44}{11} = 4 \text{ times}$$

15. (b)

The operation performed by different accessing modes, write fetching the operands are as follows:

Mode	Operations
Register AM	1RR
Direct AM	1MR
Indirect AM	2MR
Register Indirection	1RR and 1MR
Indexed AM	1RR and 1 MR and 1 ALU

Average fetch time = $\Sigma(\text{frequency} \times \text{Cycle consumed per mode})$
 $= (0.25 \times 2MR) + (0.30 \times 1MR) + (0.20 \times 1RR) + (0.15 \times (1RR + 1MR)) + (0.10 \times (1RR + 1MR + 1ALU))$
 $= (0.25 \times 16) + (0.30 \times 8) + (0.20 \times 0) + (0.15 \times 8) + (0.10 \times 12) = 8.8 \text{ cycles}$

Now, frequency = 500 MHz

Cycle time = $1/500 = 2 \text{ nsec}$

Average operand fetch time = $8.8 \times 2 \text{ nsec}$

= 17.6 nsec

So, one operand fetch require 17.6 nsec time

then, no of operand fetched in 1 sec = $\frac{1}{17.6} \times 10^9 = 56.8 \text{ MIPS}$

16. (5)

Assume that pipeline stages are IF, ID, EX, MEM, WB.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I_1	IF	ID	EX	MEM	WB										
I_2		IF	ID	EX	MEM	WB									
I_3			IF	—	ID	EX	MEM	WB							
I_4					IF	—	—	ID	EX	MEM	WB				
I_5								IF	ID	—	—	EX	MEM		
														WB	

Number of cycles to complete is 14 and the stall cycles are 5. So, answer is 5.

17. (b)

Execution time for Pipeline

$$= (K + n - 1) \times \text{execution_time}$$

Where, k = Number of stages in pipeline

n = Number of instructions execution time

= Max (all stages execution time)

$$D_1 = (5 + 100 - 1) \times 4 = 416$$

$$D_2 = (8 + 100 - 1) \times 2 = 214$$

Time saved using:

$$D_2 = 416 - 214 = 202$$

18. (78)

4 memory references \rightarrow 1 Instruction

1000 memory references \rightarrow ? instructions.

$$\text{Number of instructions} = \frac{1000}{4} = 250$$

$$\left[\frac{\# \text{ memory stalls}}{\# \text{ Instructions}} \right] = \left[\frac{\# \text{ misses } L_1}{\# \text{ Instructions}} \times \text{hit } L_2 \right] + \left[\frac{\# \text{ misses } L_2}{\# \text{ Instructions}} \times \text{miss penalty } L_2 \right]$$

$$= \left[\frac{150}{250} \times 50 \right] + \left[\frac{100}{250} \times 120 \right] = [30 + 48] = 78 \text{ cycles}$$

19. (d)

Throughput \times Number of stages \Rightarrow 1 is true

Latency will be less for M-7 \Rightarrow 2 is true

Since, the throughput is higher for M-7, program will execute faster than that on M-5 \Rightarrow 3 is true.