POSTAL Book Package 2021

Electronics Engineering

Conventional Practice Sets

Computer Organization and Architecture

Contents

MADE EASY Publications

1 CHAPTER

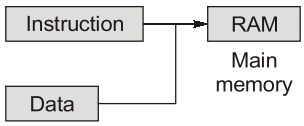
Computer Organization

Practice Questions : Level-I

Q.1 Describe computer block diagram and list its internal components.

Solution:

Computer is a computational machine, used to process data under the control of a program. Computer system is implemented using Von Neumann architecture which says that instruction and data both are present in main memory.



Computer system contains 3-fundamental components:

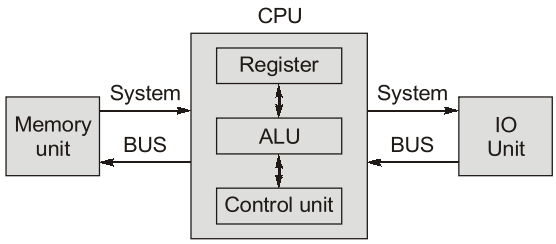
(i) **Central Processing Unit (CPU) :** . It contains 3 internal components
→ Registers → ALU → Control unit.

(ii) **Memory:** It is the storage component of computer. Memory chip is organised into cells called as addressable unit.

Ex: 64 KB RAM = 64 K × B → Cell Size
↓
Cells in chip

(iii) **IO:** It is external communication unit. It is of two kind as

(a) Input devices ($\overline{IORD}$) (b) Output devices ($\overline{IOWR}$)



Q.2 Explain different instruction format possible in computer design.

Solution:

CPU organisation is classified into 3-type:

(i) **Stack CPU :** In this organisation ALU operations are performed only on a stack data means both of the operands are always present in stack. After processing result is also present in stack.

(ii) **Accumulator CPU :** In this organisation ALU's 1st operand is always required in the accumulator and 2nd operand is present either is register or memory.
After processing result is always present in accumulator.

(iii) Register CPU :

(a) Register to memory reference CPU: In this organisation ALU 1st operand is always required in register and 2nd operand is present either in register or in memory. After processing result is placed in source-1 register.

(b) Register to register reference CPU: In this organisation, ALU operations are performed only on register data, means both of the operands are always required in register. After processing result in placed in 3rd register.

Q.3 List five distinct features each of the RISC based and the CISC based design of processors.

Solution:

RISC (Reduced Instruction Set Computer)	CISC (Complex Instruction Set Computer)
It requires multiple clock per instruction.	It requires one clock cycle per instruction.
More number of instruction	Less number of instruction.
More addressing modes	Few addressing mode.
It is hardwired.	It is micro programmed.
It is slower.	It is faster.

Q.4 Distinguish between

(i) High level language and low level language
(ii) Macro-Programming and Micro-Programming
(iii) Machine cycle and instruction cycle
(iv) Hardware interrupt and software interrupt
(v) Memory mapped I/O and I/O mapped I/O

Solution:

(i) Machine specific languages are known as low level language **e.g.** machine language and assembly languages are low level language.

While machine independent languages are high level language **e.g.** C, C++, JAVA, PASCAL.

(ii) Image's built in programming languages can be used to automate complex or repetitive task in case of microprogramming. Microcode is a layer of hardware level instruction and writing microcode is called as microprogramming. Macro instruction is a statement typically for an assembler that invokes a macro definition to generate a sequence of instructions. While microinstruction is hardware level instruction used for implementation of machine code.

(iii) Machine cycle is defined as cycle for accessing memory one time.

While instruction cycle is defined as cycle (total T states) required for execution of an instruction. An instruction cycle contains several machine cycles. **e.g.** MVI M, 20 H contains 3 machine cycle → 1 op-code fetch + 1 read + 1 write.

(iv) A hardware interrupt causes the processor to save its state of execution and begin execution of an interrupt handler.

Software interrupts are usually implemented as instructions in the instruction set, which causes a context switch to an interrupt handler similar to hardware interrupt.

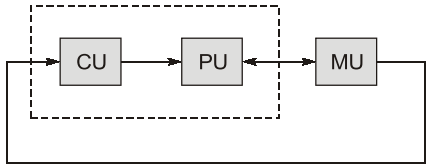
Trigger for hardware interrupt is a electrical signal while for software it is execution of machine language instruction.

(v) In memory mapped I/O address is of 16 bit while in I/O mapped i/o address is of 8 bit. All memory related instructions are used in memory mapped I/O while IN and OUT instructions are only used in case of I/O mapped. Arithmetical or logical operations can be directly performed in case of memory mapped I/O with I/O data while it is not possible in case of I/O mapped.
In case of memory mapped i/o memory is shared between I/Os and system memory. While I/O mapped is independent of memory map.
In case of memory mapped more hardware needed compare to that of i/o mapped I/O.

Q.5 Explain Flynn's classification of computer design?

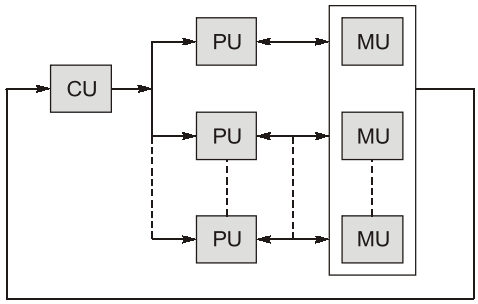
Solution:

(a) **Single Instruction Single Data (SISD) :** No concurrency in this computer.



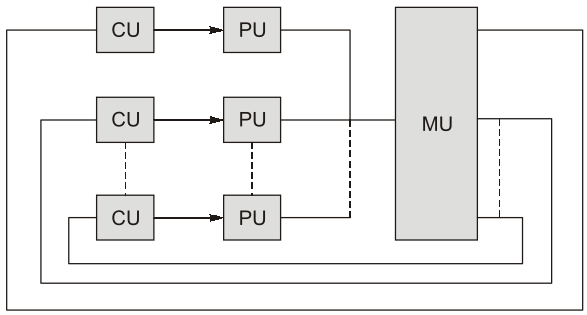
Ex : 8085

(b) **Single Instruction Multiple Data (SIMD) :** Data level concurrency is present

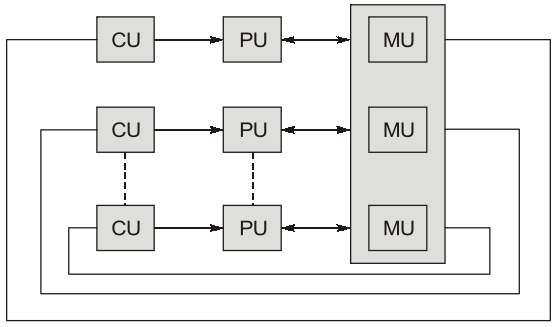


Ex : Staran processor.

(c) **Multiple Instruction Single Data (MISD) :** This architecture contains multiprocessor but only one processor is used at a time.



(d) **Multiple Instruction Multiple data (MIMD) :** This architecture contains instruction level concurrency.



Q.6 Brief about instruction pipeline and evaluate performance gain of the pipeline over non-pipeline system.

Solution:

Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction take place in a pipelines processor.

- Pipelined processor has multistage/segments such that output of one stage is connected to input of next stage and each stage performs a specific operation.
- Interface registers are used to hold the intermediate output between two stages. These interface registers are also called latch or buffer.
- All the stages in a pipeline along with the interface registers are controlled by a common clock.

Performance of a pipelined processor:

Consider a k segment pipeline with clock cycle time as 'T_P'. Let there be 'n' tasks to be completed in the pipelined processor.

Now, the first instruction will take 'k' cycles to come out of the pipeline but the other $n-1$ instructions will take only one cycle each. i.e. a total of $(n-1)$ cycles. So, time taken to execute 'n' instructions in a pipelined processor:

$$ET_{\text{pipeline}} = (k + n - 1) \text{ cycles}$$
$$= (k + n - 1)\, T_P$$

For a non-pipelined processor, execution time of 'n' instructions will be

$$ET_{\text{non-pipeline}} = n * k * T_P$$

So, speed up (S) of the pipelined processor over non-pipelined processor, when 'n' tasks are executed on the same processor is

$$S = \frac{ET_{\text{non-pipeline}}}{ET_{\text{pipeline}}}$$

$$S = \frac{(n \times k \times T_P)}{(k + n - 1)T_P} = \frac{n \times k}{(k + n - 1)}$$

When number of tasks 'n' are larger than k,

i.e. $n >> k$

$$S_{\max} = \frac{n \times k}{n} = k$$

$$S_{\max} = k$$

$$\text{Efficiency} = \frac{\text{Given speed up}}{\text{Max. speed up}}$$

$$\eta = \frac{S}{S_{\max}} = \frac{S}{k}$$

Q.7 Compare Hard-wired CU and microprogrammed CU design.

Solution:

Sl. No.	Hardwired Control Unit	Micro programmed Control Unit
1.	It is a sequential circuit that generate control signals. It uses a fixed architecture.	It is a unit with micro instructions in the control memory to generate control signals.
2.	The speed of operation is fast.	The speed of operations is slow because it requires frequent memory access.
3.	To do modification, entire unit should be redesigned.	Modification can be implemented by changing the micro instructions in the control memory.
4.	It is more costly to implement.	It is less costly to implement.
5.	It is difficult to perform instruction decoding.	Instruction decoding is easier.
6.	It uses small instruction set.	It uses large instruction set.
7.	There is no control memory usage.	It uses control memory.
8.	It is used in processors that use a simple instruction set known as the reduced instruction set computer (RISC).	This control unit is used in processors based on complex instruction set known as complex instruction set computer (CISC)

Q.8 Differentiate between horizontal programming and vertical programming of microprogrammed control unit.

Solution:

Horizontal Programming	Vertical Programming
1. In this control signal is expressed in a decoded binary format.	1. In this control is expressed as encoded format.
2. It supports longer control word.	2. It supports shorter control word.
3. No need of external decoder.	3. External decoder needed.
4. It is comparatively faster.	4. It is comparatively slower.
5. High degree of parallelism.	5. Low degree of parallelism.

Q.9 In view of important parameters, give the comparison between RAM and ROM in tabular form.

Solution:

Comparison between RAM and ROM

Parameter	RAM	ROM
1. Data storage	Temporary. Vanishes when power is switched off.	Permanent power failure does not affect data stored.
2. Data entry	Data can be entered fast. No Special program-writers are required.	Special program-writers are required.So, data entry is normally slow. But this is being rectified.
3. Data read out	Data is read-out at the same time it is entered.	Data read-out only after it is entered.
4. Repeatability of read out	Once the data is erased, it cannot be recovered.	Data is not erased; hence, it can be read out any number of times.
5. Erasability	Easily, erasable, very fast operation.	Not easily erasable, slower operation.
6. Packing density	Currently large.	Currently low.
7. Static/dynamic operations	Static and dynamic operation exist.	Only static ROMs exist.
8. Use of memory	Data entered in any computer is first stored in RAM. If the data is to be stored permanently it will be saved in the hard disk.	This memory stores data of a permanent nature such as operating-system commands, look-up tables, etc., which are not stored in hard disks.

Practice Questions : Level-II

Q.10 Bring out the concept of virtual memory and briefly point out its operation.

Solution:

Virtual Memory:

- Virtual memory is a memory management capability of an OS that uses hardware and software to allow a computer to compensate for physical memory shortages by temporarily transferring data from RAM to disc storage.
- Virtual address space is increased using active memory in RAM and inactive memory in hard disk drives to form contiguous addresses that hold both the application and its data.
- Virtual memory concept is implemented using:
  (i) Paging
  (ii) Segmentation

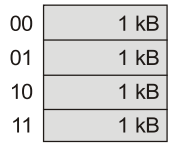
  Paging:
  - In this technique, main memory and secondary memory both are divided into a equal sized pages based on the page size.
  - After the organization memory cells are grouped into a frames in main memory and pages in secondary memory.

$$\#\text{ Frames in main memory (MM)} = \frac{\text{MM size}}{\text{Page size}}$$

$$\#\text{ Pages in secondary memory (SM)} = \frac{\text{SM size}}{\text{Page size}}$$

- Consider 8 kB secondary space and 4 kB main memory space organized into a 1 kB pages.

$$\#\text{ Frames} = \frac{4\,K}{1K} \Rightarrow 4$$



$$\#\text{ Pages} = \frac{8\,K}{1K} \Rightarrow 8$$