Electronics Engineering

Digital Circuits

Comprehensive Theory

with Solved Examples and Practice Questions

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Corporate Office: 44-A/4, Kalu Sarai (Near Hauz Khas Metro Station), New Delhi-110016
E-mail: infomep@madeeasy.in
Contact: 011-45124612, 0-9958995830, 8860378007

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CHAPTER 6

Synthesis of Synchronous Sequential Circuits

Introduction

State Diagram (State graph)

It is a pictorial representation of the relationships between the present state, the input, the next state and the output of a sequential circuit, i.e. the state diagram is a pictorial representation of the behaviour of a sequential circuit.

State table

The state table is a tabular representation of the state diagram. Even though the behaviour of a sequential circuit can be conveniently described using a state diagram, for its implementation the information of the state diagram is to be translated into a state table. Both the state diagram and the state table contain the same information.

6.1 Finite State Machine (FSM)

- Finite state machines are sequential circuits whose past histories can affect their future behaviour in only a finite number of ways, i.e. they are machines with a fixed number of states.
- A sequential circuit is referred to as a finite state machine (FSM).
- Finite state machines are of two types. They differ in the way the output is generated. They are
  1. Mealy type model 2. Moore type model

6.1.1 Mealy Machine

In this model, the output depends on both the present state of the circuit and the present inputs.

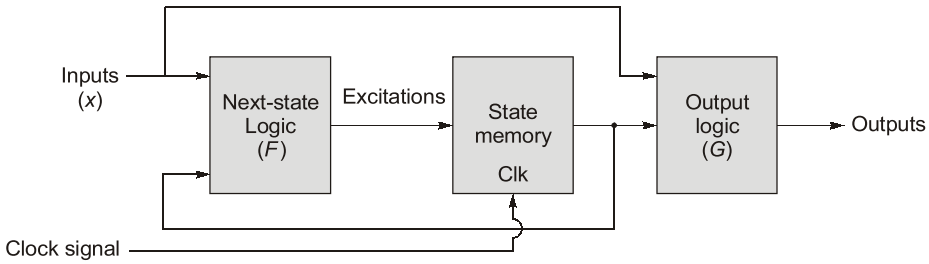
$$NS = F(PS, X)$$
$$Output = G(PS, X)$$

F and G are some logic functions.

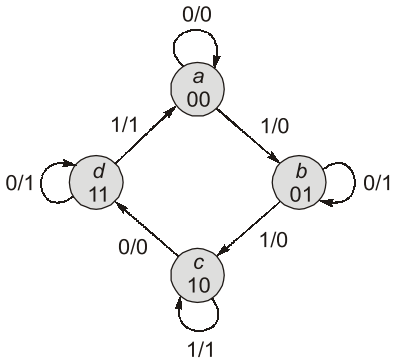
PS = Present state
NS = Next state
X = Present inputs

Input changes may affect the output of the logic circuit.

It requires less number of states for implementing a function than that of Moore model.



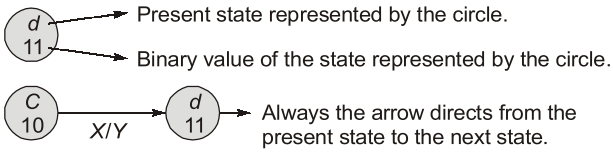
State diagram and state table for a Mealy circuit are given below.



State diagram

PS	NS output	
	$X = 0$	$X = 1$
a	a, 0	b, 1
b	b, 1	c, 0
c	d, 0	c, 1
d	d, 0	a, 1

Stable table



X = Input and Y = Output

In the Mealy model, the output depends on the present input. Hence both input, output are represented on the directed lines.

6.1.2 Moore Machine

In this model, the output depends only on the present state of the circuit.

$$NS = F(PS, X)$$

$$Output = G(PS)$$

F and G are some logic functions.

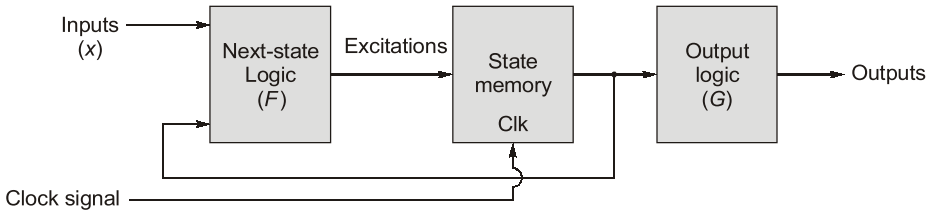
PS = Present state

NS = Next state

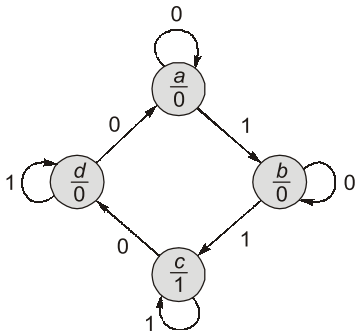
X = Present inputs

Input changes do not affect the output of the logic circuit.

It requires more number of states for implementing a function than that of Mealy model.



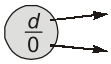
State diagram and state table for a Moore circuit are given below.



State diagram

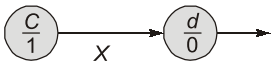
PS	NS Input		Present output
	$X = 0$	$X = 1$	
a	a	b	0
b	b	c	0
c	d	c	1
d	a	d	0

State table



Present state represented by the circle.

Output of the circuit corresponding to the present state represented by the circle.

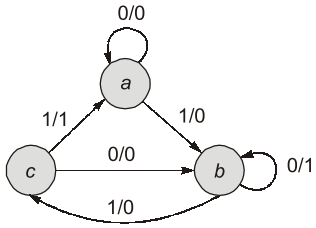


Always the line directs from the present state to the next state.

X = Input

In the Moore model, the output depends only on the present state of the circuit and it is independent of the input applied. Hence, the present output is represented inside the circle belongs to the present state and input is represented on the directed line.

Example - 6.1 Draw the equivalent Moore state diagram for the following Mealy state diagram.



Solution :

In a Moore state diagram, each state is associated with a fixed output.

States for the Moore state diagram, corresponding to the given Mealy stae diagram, can be assigned as shown below.

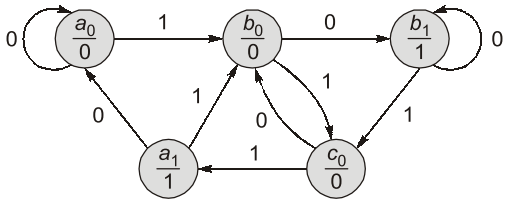
Mealy State	Equivalent Moore State
a, with output 0	a_0
a, with output 1	a_1
b, with output 0	b_0
b, with output 1	b_1
c, with output 0	c_0

In the given Mealy state diagram, there no transition that produces next state as "c" with output "1". Hence, there is no need a state equivalent to "c" with output "1", i.e. c_1 in Moore model.

The state table and state diagram of the required Moore model can be given as,

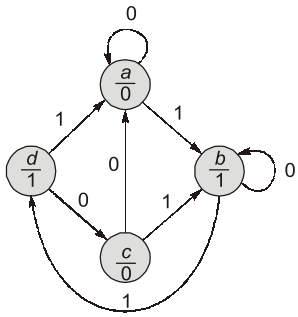
Present state	Next state (output)	
	$X = 0$	$X = 1$
a_0	$a_0(0)$	$b_0(0)$
a_1	$a_0(0)$	$b_0(0)$
b_0	$b_1(1)$	$c_0(0)$
b_1	$b_1(1)$	$c_0(0)$
c_0	$b_0(0)$	$a_1(1)$

State table



State diagram

Example - 6.2 Draw the equivalent Mealy state diagram for the following Moore state diagram.



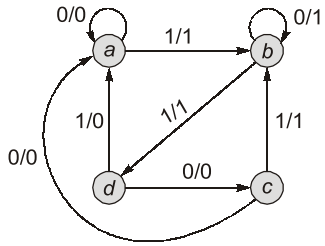
Solution :

Same state notations can be followed in the corresponding Mealy state diagram of the given Moore state diagram.

The state table and state diagram of the required Mealy model can be given as,

Present state	Next state		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	b	0	1
b	b	d	1	1
c	a	b	0	1
d	c	a	0	0

State table

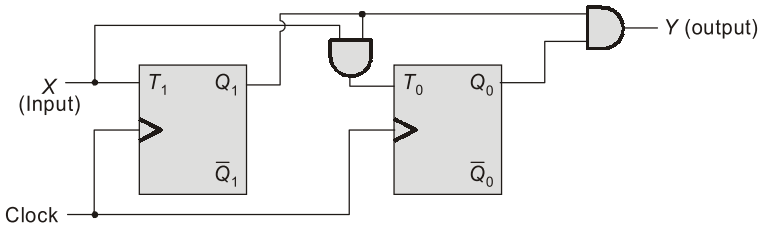


State diagram

State Reduction

- The state reduction technique basically avoids the introduction of redundant states.
- The reduction in redundant states reduces the number of flip-flops and logic gates, reducing the cost of the final circuit.
- Two states are said to be equivalent if every possible set of inputs generate exactly the same output and the same next state.
- When two state are equivalent, one of them can be removed without altering the input-output relationship.
- Let us illustrate the reduction technique with an example.

Example - 6.3 Develop a state diagram for the logic circuit shown in the figure below.



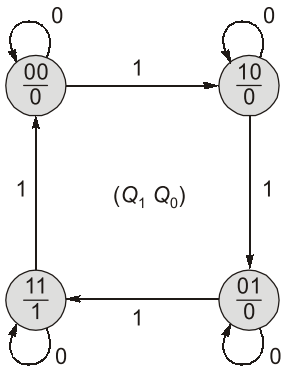
Solution :

Excitations of the flip flops are, $T_1 = X$ and $T_0 = Q_1X$

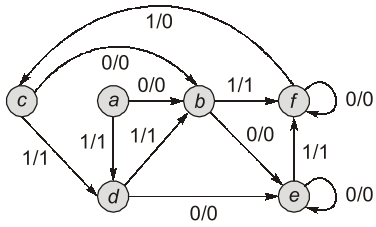
Output signal, $Y = Q_1Q_0 \Rightarrow$ Moore circuit

The state table and state diagram of the given sequential circuit can be developed as shown below.

Present state		Input	Excitations		Next state		Output
Q_1	Q_0	X	T_1	T_0	Q_1^+	Q_0^+	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	1	1	0	1	1	1
1	0	0	0	0	1	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	0



Example - 6.4 Reduce the following state diagram:



Solution :

- The state table of the given state diagram is,

PS	NS		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	b	d	0	1
b	e	f	0	1
c	b	d	0	1
d	e	b	0	1
e	e	f	0	1
f	f	c	0	0

"*b*" and "*e*" are said to be equivalent states. So, remove "*e*" and replace it with "*b*".

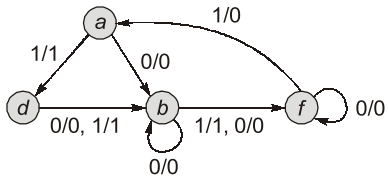
"*a*" and "*c*" are said to be equivalent states. So, remove "*c*" and replace it with "*a*".

- So, the reduced state table is,

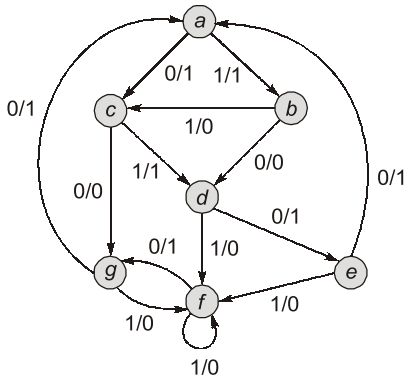
PS	NS		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	*b*	*d*	0	1
b	*b*	*f*	0	1
d	*b*	*b*	0	1
f	*f*	*a*	0	0

No further equivalent states are found. So, it is not possible to reduce further.

- Now, the reduced state diagram can be drawn from the reduced state table as shown below:



Example - 6.5 Reduce the following state diagram:



Solution :

- The state table of the given state diagram is,

PS	NS		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	*c*	*b*	1	1
b	*d*	*c*	0	0
c	*g*	*d*	0	1
d	*e*	*f*	1	0
e	*a*	*f*	1	0
f	*g*	*f*	1	0
g	*a*	*f*	1	0

"*g*" and "*e*" are said to be equivalent states. So, remove "*g*" and replace it with "*e*".

- The reduced state table is,

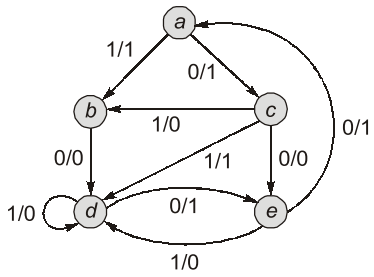
PS	NS		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	c	b	1	1
b	d	c	0	0
c	e	d	0	1
d	e	f	1	0
e	a	f	1	0
f	e	f	1	0

"e" and "f" are said to be equivalent states. So, remove "f" and replace it with "e".

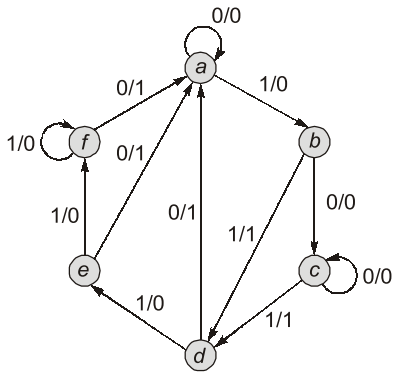
- The reduced state table is,

PS	NS		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	c	b	1	1
b	d	c	0	0
c	e	d	0	1
d	e	d	1	0
e	a	d	1	0

- No further reduction is possible, hence the reduced state diagram is as shown below:



Example - 6.6 Reduce the following state diagram:



Solution :

- The state table of the state diagram can be given as follows:

Present State	Next State $X=0$	Next State $X=1$	Output $X=0$	Output $X=1$
a	a	b	0	0
b	c	d	0	1
c	c	d	0	1
d	a	e	1	0
e	a	f	1	0
f	a	f	1	0

X = Input

States "b" and "c" have same next state and output for a given value of input. So, these two states are said to be equal and we can replace the state "c" with state "b".

States "e" and "f" have same next state and output for a given value of input. So, these two states are said to be equal and we can replace the state "f" with state "e".

- After replacing states "c" and "f" with states "b" and "e" respectively, the resultant state table is as follows:

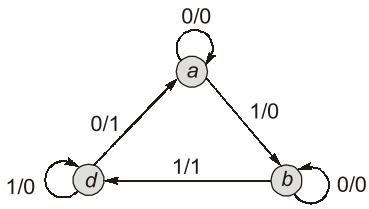
Present State	Next State $X=0$	Next State $X=1$	Output $X=0$	Output $X=1$
a	a	b	0	0
b	b	d	0	1
d	a	e	1	0
e	a	e	1	0

States "d" and "e" have same next state and output for a given value of input. So, these two states are said to be equal and we can replace the state "e" with state "d".

- After replacing state "e" with state "d", the resultant state table is as follows:

Present State	Next State $X=0$	Next State $X=1$	Output $X=0$	Output $X=1$
a	a	b	0	0
b	b	d	0	1
d	a	d	1	0

- In the above state table, no two states have same next state and output for a given value of input. Hence there are no equal states and it is not possible to reduce the state table further.
- From the above table, the reduced state diagram of the given state diagram can be drawn as follows:



Example - 6.13 Develop Mealy and Moore type of state diagrams for a one input-one output sequence detector, to detect the sequence "110011".

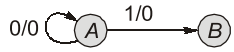
Solution :

For Mealy model design

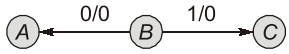
For Mealy model, the number of unique states = number of bits in the sequence to be detected.
In this question, the sequence to be detected is "11011".
Number of bits in the sequence = 5 $\Rightarrow$ Number of unique states = 5 (let us say A, B, C, D, E)

If overlapping sequences are not allowed to detect:

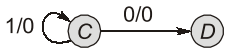
$A : X \Rightarrow$ if $X = 0 \Rightarrow$ Remains in the state A; if $X = 1 \Rightarrow$ Moves to the state B } in both cases o/p = 0



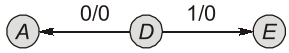
$B : 1\ X \Rightarrow$ if $X = 0 \Rightarrow$ Moves to the state A; if $X = 1 \Rightarrow$ Moves to the state C } in both cases o/p = 0



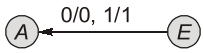
$C : 1\ 1\ X \Rightarrow$ if $X = 0 \Rightarrow 110 \Rightarrow$ Moves to the state D; if $X = 1 \Rightarrow 111 \Rightarrow$ Remains in the state C } in both cases o/p = 0



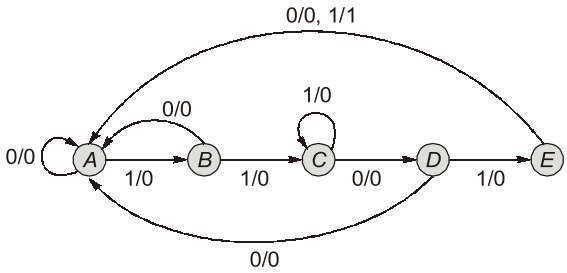
$D : 1\ 1\ 0\ X \Rightarrow$ if $X = 0 \Rightarrow 1100 \Rightarrow$ Moves to the state A; if $X = 1 \Rightarrow 1101 \Rightarrow$ Moves to the state E } in both case o/p = 0



$E : 1\ 1\ 0\ 1\ X \Rightarrow$ if $X = 0 \Rightarrow 11010 \Rightarrow$ Moves to the state $A \Rightarrow$ o/p = 0; if $X = 1 \Rightarrow 11011 \Rightarrow$ Moves to the state $A \Rightarrow$ o/p = 1



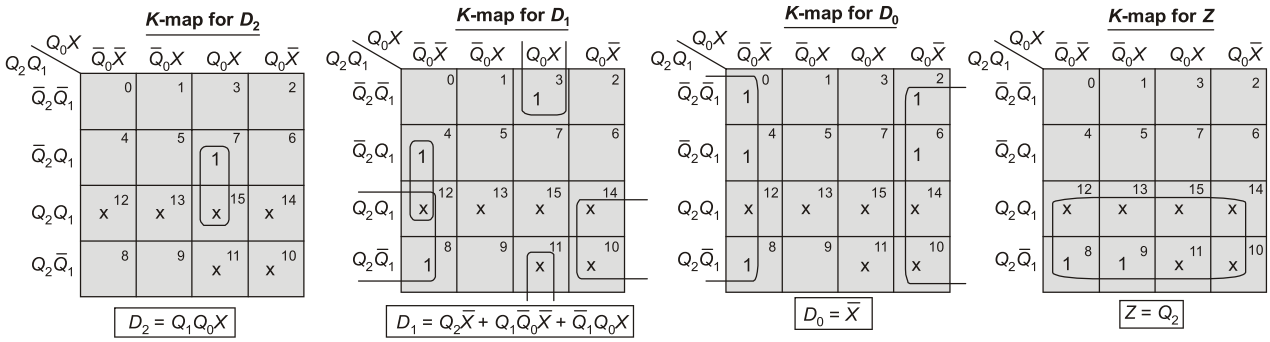
As overlapping is not permitted, after the detection of the desired sequence, the machine moves to the first state.
The resulting state diagram is,



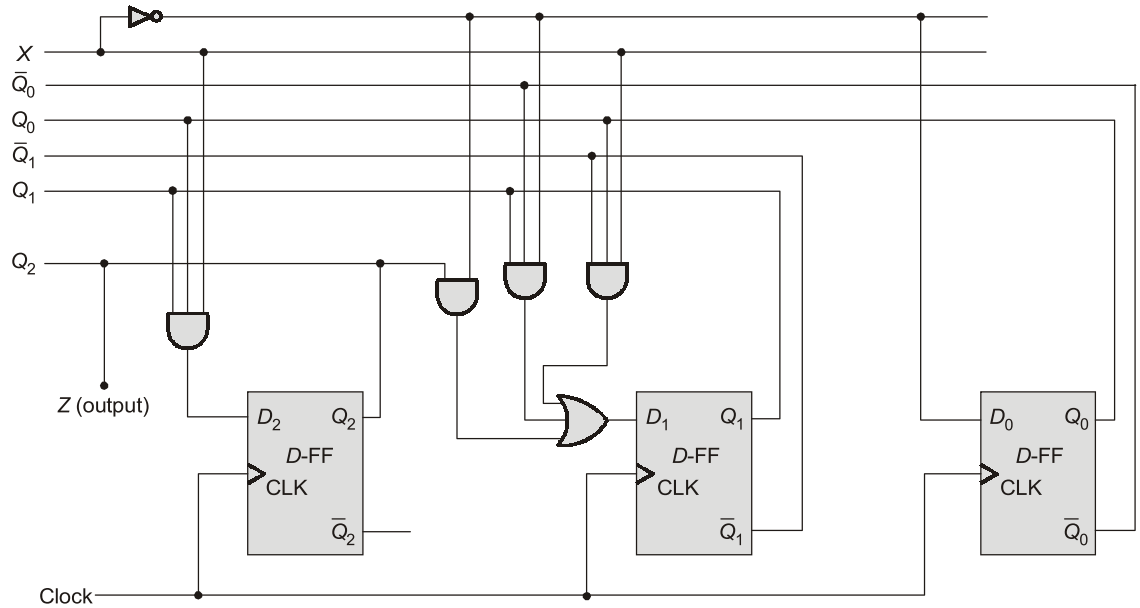
If overlapping sequences are allowed to detect:

For the overlapping case, the state transitions from the states A, B, C, D are same as that of the non-overlapping case. Only the state transitions from the state E will change as follows,

Minimization :

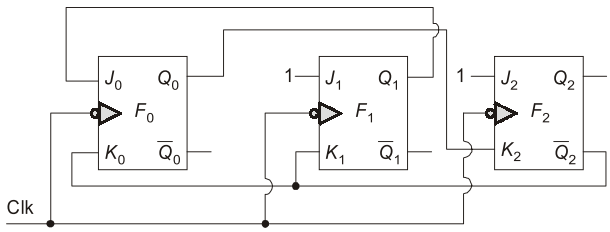


Logic circuit :

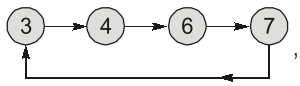


Student's Assignments 1

Q.1 Consider the counter circuit shown in the figure below:



The counter is designed such that it counts the states



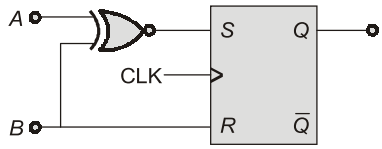
then which of the following statements about this counter is true?

(a) The counter enters into a lockout state if the counter starts from $(5)_{10}$

(b) The counter enters into a lockout state if the counter starts from $(2)_{10}$

(c) The counter enters into a lockout state if the counter starts from $(3)_{10}$

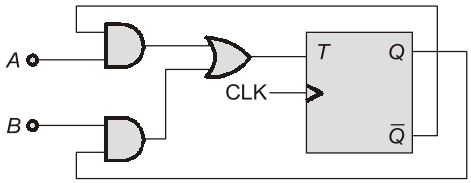
(d) The counter do not enters into a lockout state.



(a) $\bar{A}\bar{B}+AQ$ (b) $\bar{A}\bar{B}+\bar{B}Q$

(c) Both A and B (d) None of above

Q.7 What is represented by digital circuit given below?



(a) An S-R flip-flop with $A = S$ and $B = R$

(b) A J-K flip-flop with $A = K$ and $B = J$

(c) A J-K flip-flop with $A = J$ and $B = K$

(d) An S-R flip-flop with $A = R$ and $B = S$

ANSWERS

1. (d) 2. (c) 3. (d) 4. (a) 5. (c)
6. (c) 7. (c & a)

Student's Assignments 2

Q.1 Design a 4-bit serial-in, serial-out, bidirectional shift register using D-flip flops. The design should consist a mode control bit 'M'. When $M = 0$, the register should work as shift-left shift register and when $M = 1$, the register should work as shift-right shift register.

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