Electrical Engineering

Digital Electronics

Comprehensive Theory

with **Solved Examples** and **Practice Questions**

MADE EASY
Publications

MADE EASY Publications

Corporate Office: 44-A/4, Kalu Sarai (Near Hauz Khas Metro Station), New Delhi-110016
E-mail: infomep@madeeasy.in
Contact: 011-45124612, 0-9958995830, 8860378007
Visit us at: www.madeeasypublications.org

Digital Electronics

First Edition: 2015
Second Edition: 2016
Third Edition: 2017
Fourth Edition: 2018
Fifth Edition: 2019
Sixth Edition: 2020

Contents

Digital Electronics

CHAPTER 7

A/D and D/A Converters

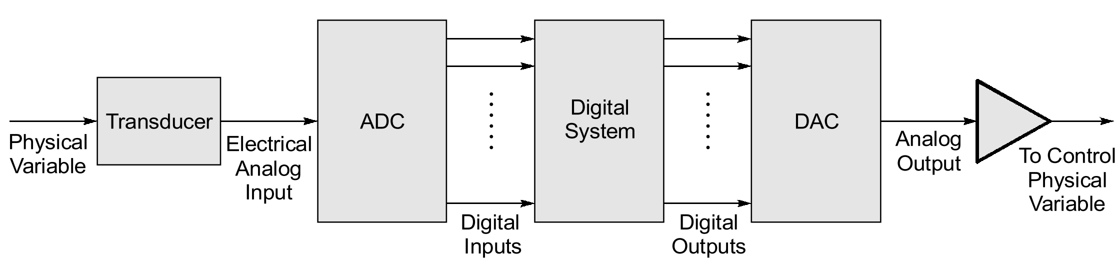
Introduction

In practical world most of the physical variables are analog in nature and can take on any value within a continuous range of values for example temperature, pressure, light intensity, audio signals etc. However, the digital systems perform all of their internal operations using digital circuitry. Any information that has to be input to a digital system must first be converted into digital form and the outputs are always in digital form. Therefore, the interfacing of analog and digital systems requires the data (signal) to be co
nverted from one form to other.

The process of converting an analog signal to a digital form involves the sequence of four processes:

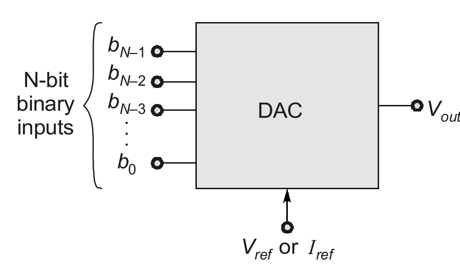
1. Sampling
2. Holding
3. Quantizing
4. Encoding

Here, 'sampling' and 'holding' operations are done simultaneously using a circuit known as **sample-and-hold circuit (S/H).** The 'Quantizing' and 'Encoding' processes are done simultaneously using a circuit referred to as an "Analog to digital converter" (A/D converter or ADC). Now, the digital output has to be converted back to the analog form referred to as a "digital to analog converter" (D/A converter or DAC).



7.1 Digital to Analog Converter

- The digital to analog conversion is a process of taking a value represented in digital code and converting it to a voltage or current which is proportional to the digital value. The input given to the converter is an n-bit binary signal available in parallel form.



General block diagram of DAC

- The analog output voltage V_0 of an n-bit straight binary D/A converter is related to the digital input by the equation.

$$\boxed{V_0 = K\left[2^{n-1}b_{N-1} + 2^{N-2}b_{N-2} + 2^{N-3}b_{N-3} + \ldots\ldots + 2b_1 + b_0\right]}$$

or, analog output = ($K \times$ Decimal equivalent of digital input)

Where, K = Proportionality factor

b_N = 1; if the N^{th} bit of digital input is '1'

b_N = 0; if the N^{th} bit of digital input is '0'

Example - 7.1 What is the largest value of output from an 8 bit DAC that produces 1 V for a digital input of 00110010?

Solution:

$$(00110010) = (50)_{10}$$

$$\therefore \quad 1\text{ V} = K \times 50 \quad \Rightarrow \quad K = 20\text{ mV}$$

The largest output will occur for an input of $(11111111)_2 = (255)_{10}$

$$V_{out(max)} = 20\text{ mV} \times (255)_{10} = 5.10\text{ V}$$

Type of D/A converters

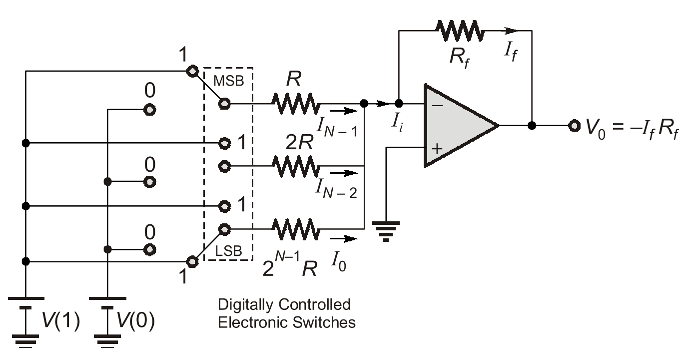
There are two types of commonly used D/A converters. These are:

(i) Weighted Resistor DAC

(ii) $R - 2R$ ladder DAC

7.1.1 Weighted Resistor D/A Converter

As the conversion from digital to analog signal involves a weighted sum corresponding to the input of the converter, the circuit given below can be used for the conversion.



Weighted Resistor DAC

In the circuit given above, since the resistance values are weighted in accordance with the binary weight, so it is called 'Weighted resistor D/A converter'. Here Op-amp is employed as 'summing amplifier'. In the above circuit the digital input (1 or 0) operate the switches. A switch is thrown to position 1 or 0 for a digital input corresponding to that bit being 1 or 0, respectively position '0'. The voltage applied to a resistor is V (1) if the switch connected to it, in position '1' and V (0) if it is in position '0'.

The current I_i is given by:

$$I_i = I_{N-1} + I_{N-2} + I_{N-3} + \ldots\ldots + I_0$$

Where,

$$\left.\begin{aligned} I_{N-1} &= \frac{V_{N-1}}{2^0 \cdot R} \\ I_{N-2} &= \frac{V_{N-2}}{2^1 \cdot R} \\ I_{N-3} &= \frac{V_{N-3}}{2^2 \cdot R} \\ &\vdots \\ I_0 &= \frac{V_0}{2^{N-1} \cdot R} \end{aligned}\right\}$$

Where,
$V_N = V(1);$ if $b_1 = 1$
$= V(0);$ if $b_0 = 0$

Since, Op-Amp output $V_0 = -I_i R_F$
for straight binary input, $V(0) = 0$ and $V(1) = -V_R$

$\therefore$ The output voltage,

$$V_0 = -(-V_R)\left[\frac{R_F}{R} \cdot b_{N-1} + \frac{R_F}{2R} b_{N-2} + \ldots.. \frac{R_F}{2^{N-1} R} b_0\right]$$

$$V_0 = \frac{R_F}{2^{N-1} R} \cdot V_R \cdot [b_{N-1} + b_{N-2} + b_{N-3} + \ldots.. + b_0]$$

In the above equation the proportionality factor can be given as,

$$K = \frac{R_F}{2^{N-1} \cdot R} \cdot V_R$$

and

$$V_0 = \frac{R_F}{2^{N-1} \cdot R}\left(2^{N-1} V_{N-1} + 2^{N-2} V_{N-2} + \ldots.. + 2^0 V\right)$$

- The Op-Amp in the above figure is operated in inverting mode to work as an excellent **"Current-to-Voltage Converter"**.

  where,

$$I_i = \frac{V_R}{2^{N-1} R} \cdot \left[2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \ldots.. + 2^0 b_0\right]$$

  or

$$I_i = \frac{V_R}{2^{N-1} R} \sum_{i=0}^{N-1} 2^i b_i$$

- The maximum output current will flow when all b_i coefficients are '1'.

  i.e.

$$\boxed{(I_i)_{\max} = \frac{V_R}{2^{N-1} R} \cdot (2^{N-1})}$$

NOTE

- LSB Resistance = (2^{N-1}) × MSB Resistance.
- Typical value of resistance R ranges from 2.5 kΩ to 10 kΩ.

Disadvantage of Weighted-Resistor Type DAC

Weighted-resistor type DAC has several disadvantages which are as follows:

(*i*) When number of input bits is large, the resistance used for LSB has very large value.

(*ii*) Due to the large difference in resistance values between the LSB and MSB, we cover a wide range of resistances tracking of which over a wide temperature range is difficult to produce.

(*iii*) Due to the "Loading effect" (input impedance will not remain constant), accuracy of the system is less.

(*iv*) Linearity is less.

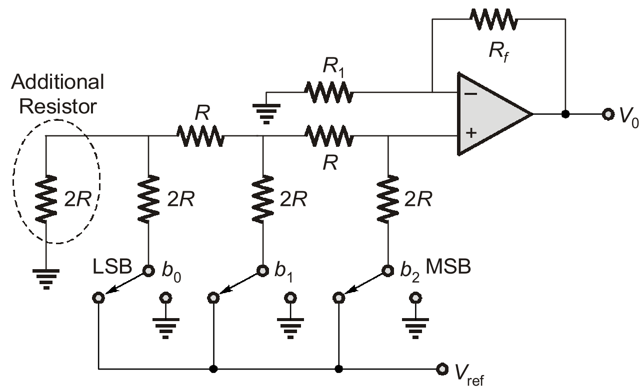
7.1.2 R-2R Ladder DAC

The *R*-2*R* ladder DAC is further classified as:

- Normal ladder type
  (*i*) Non-inverting OP-AMP Type (*ii*) Inverting OP-AMP type
- Inverted ladder type
- Switch capacitor type

R-2R Ladder DAC by using Non-inverting OP-AMP

- An *R*-2*R* ladder DAC uses resistors of only two values *R* and 2*R*. The input to the resistor is applied through digitally controlled switches.
- To analyze this circuit consider a 3-bit *R*-2*R* ladder DAC as shown in figure below.



***R*-2*R* Ladder DAC (using non-inverting Op-amp)**

For a non-inverting op-amp

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \left(1+\frac{R_F}{R_1}\right)$$

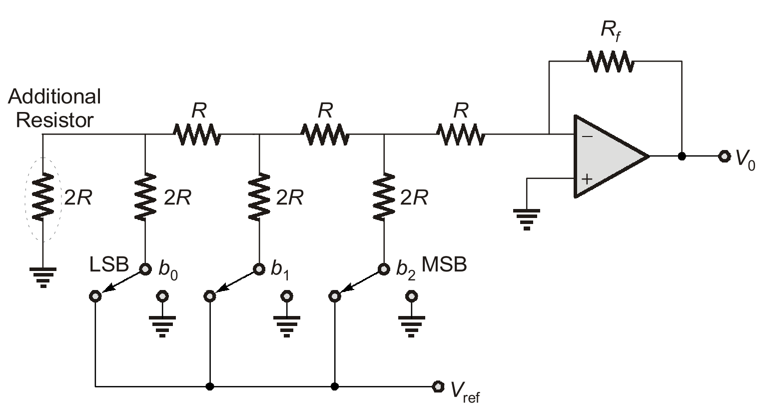
The output analog voltage V_0 is given by

$$\boxed{V_0 = \left(1+\frac{R_F}{R_1}\right)\times\left(\frac{V_{ref}}{2^N}\right)\times\left(\sum_{i=0}^{N-1} 2^i b_i\right)}$$

Therefore, V_0 = (Gain) × (Resolution) × (Decimal equivalent of binary input applied)

R-2R Ladder DAC by using Inverting Op-Amp

R-2R ladder DAC with inverting Op-amp circuit is shown in the figure below.



R-2R Ladder DAC (using Inverting Op-amp)

In this circuit, we have assumed the digital input as '001' i.e. switch "S_0" is closed. This circuit is simplified using "Thevenin's theorem". Applying Thevenin's theorem at XX', YY' and ZZ', we get the circuits of Figure (a), (b) and (c) respectively.

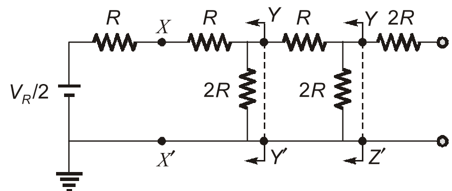


Figure (a)

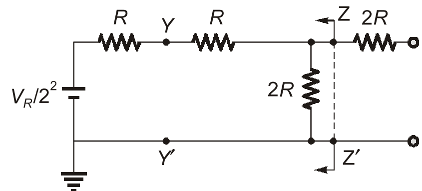


Figure (b)

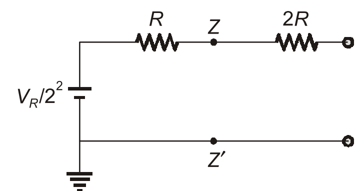


Figure (c)

Here, digital input ⇒ equivalent voltage

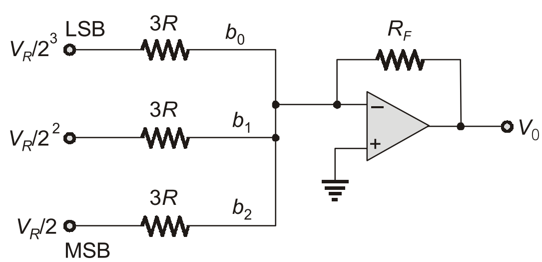
$$0\,0\,1 \Rightarrow \frac{V_R}{2^3}$$

if,

$$0\,1\,0 \Rightarrow \frac{V_R}{2^2}$$

$$1\,0\,0 \Rightarrow \frac{V_R}{2^1}$$

The value of the "input impedance" or "equivalent resistance" is $3R$ in each case. The equivalent circuit is given as,



$$V_0 = -\left(\frac{R_F}{3R}\cdot\frac{V_R}{2^3}\cdot b_0 + \frac{R_F}{3R}\cdot\frac{V_R}{2^2}\, b_1 + \frac{R_F}{3R}\cdot\frac{V_R}{2^1}\, b_2\right)$$

$$V_0 = -\left(\frac{R_F}{3R}\right)\left(\frac{V_R}{2^3}\right)[4b_2 + 2b_1 + 1b_0]$$

∵ The output voltage for n-bit DAC,

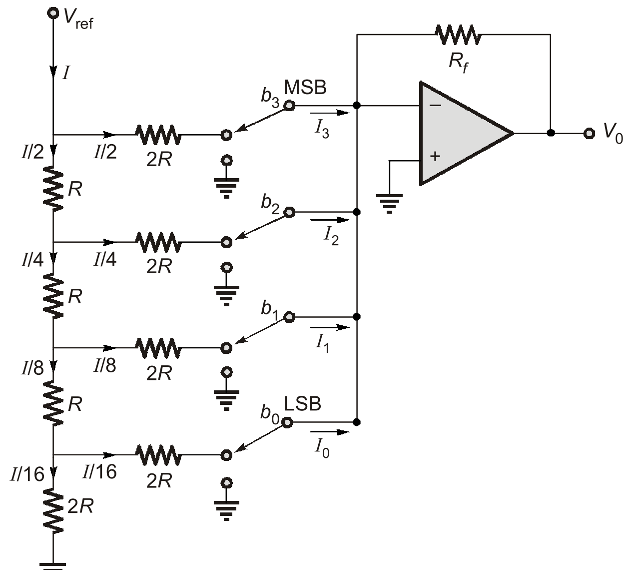
$$V_0 = (\text{Gain}) \times (\text{Resolution}) \times (\text{Decimal equivalent of binary input})$$

$$\boxed{V_0 = \left(\frac{-R_F}{R_1 + R}\right) \times \left(\frac{V_{\text{ref}}}{2^N}\right) \times \left(\sum_{i=0}^{N-1} 2^i b_i\right)}$$

Inverted R-2R Ladder DAC

In weighted resistor DAC and R-$2R$ ladder DAC (Discussed above), the current flowing through the resistors changes as the applied input changes. Thus, more power dissipation causes the heating of the circuit, which in turn produces non linearity in DAC. To avoid this problem an inverted R-$2R$ ladder type DAC is used in which current divides equally at each node irrespective of applied input. This is because the equivalent resistance to the right or to the left of any node is exactly $2R$.

The figure below shows the circuit arrangement of inverted R-$2R$ ladder type DAC. This circuit works under the principle of summing currents.



Inverted R-2R Ladder DAC

from the figure

$$I_f = \frac{-V_0}{R_f}$$

where,

$$I_f = I_3 + I_2 + I_1 + I_0 = \frac{I}{2}b_3 + \frac{I}{4}b_2 + \frac{I}{8}b_1 + \frac{I}{16}b_0$$

Therefore,

$$I_f = \frac{I}{16}\sum_{i=0}^{N-1} 2^i b_i$$

or $I_f = \dfrac{I}{2^N}\sum_{i=0}^{N-1} 2^i b_i$

and $\boxed{V_0 = \left(-\frac{R_f}{R}\right)\left(-\frac{V_{ref}}{2^N}\right)\times\left(\sum_{i=0}^{N-1} 2^i b_i\right)}$

The most important feature of inverted R-$2R$ DAC is that, since all the switches are at the same potential even with changing input binary words. The stray capacitance is not able to produce slow down effects on the performance of the circuit. The R-$2R$ ladder DAC has following advantages over weighted resistor DAC:

- The R-$2R$ DACs have better linearity.
- It requires only two different type of resistors with values R and 2R.

Note: A D/A converter which is used as a varying analog signal instead of fixed reference voltage is called a multiplying DAC.

Example - 7.2 (a) Design a 4-bit weighted resistor DAC whose full-scale output voltage is –5 V. The logic levels are 1 = +5 V and 0 = 0 V.

(b) In the above question what will be the value of output voltage when the input is 1101?

Solution:

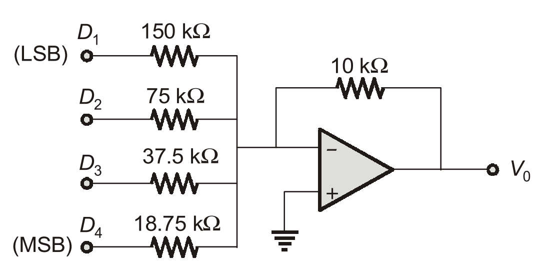
The full-scale output voltage is the output voltage when the input voltage is maximum, i.e., 1111.

$\therefore$ $$\text{Full scale output} = -\left[5\text{ V}+\frac{5\text{ V}}{2}+\frac{5\text{ V}}{4}+\frac{5\text{ V}}{8}\right]\times\frac{R_f}{R} = -5\text{ V}$$

$\therefore$ $$\frac{R_f}{R} = \frac{5}{9.357}$$

$\therefore$ Let $R_f = 10\text{ k}\Omega$

$\therefore$
$$R = 18.75\text{ k}\Omega$$
$$2R = 37.5\text{ k}\Omega$$
$$4R = 75\text{ k}\Omega$$
$$8R = 150\text{ k}\Omega$$



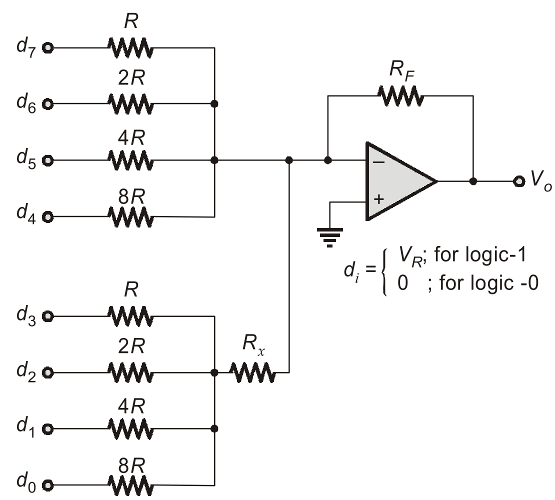
For input 1101 we will get,

$$\therefore \quad V_{out} = -\left[5\text{ V} + \frac{5\text{ V}}{2} + 0 + \frac{5\text{ V}}{8}\right] \times \frac{R_f}{R} = -8.125 \times \frac{10}{18.75} = -4.333\text{ V}$$

Example - 7.3 Consider the circuit shown in the figure below:

(i) If this circuit is to be used as an 8-bit (binary) digital-to-analog converter, then determine the relation between R_x and R.

(ii) If the same circuit is to be used as a 2-decade BCD digital-to-analog converter, then determine the relation between R_x and R, by using the calculations obtained in part (i).



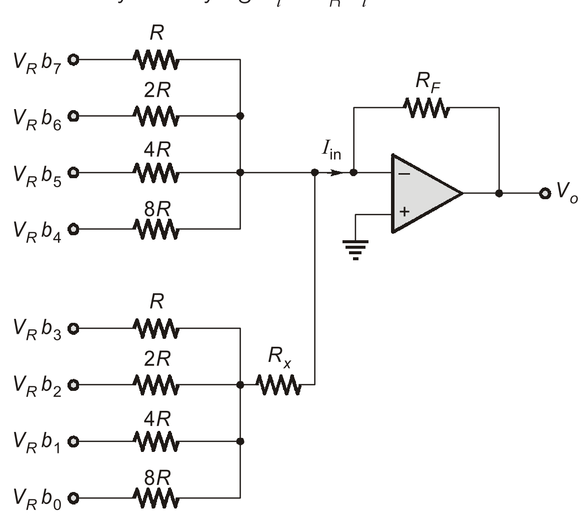
Solution:

- Let us assume that the binary logic values (1 or 0) are represented as $b_7, b_6, b_5, \ldots, b_1, b_0$.

So,
$$d_i = \begin{cases} V_R; & \text{for } b_i = 1 \\ 0\ ; & \text{for } b_i = 0 \end{cases}$$

$$d_i = V_R b_i$$

- Considering the given circuit by modifying $d_i = V_R b_i$ as shown below.



$$V_0 = -I_{in} R_F$$

- For a digital-to-analog converter,

$$V_0 \propto \text{[decimal equivalent of input binary code]}$$
$$V_0 = -I_{in}R_F$$

So, $$I_{in} \propto \text{[decimal equivalent of input binary code]}$$

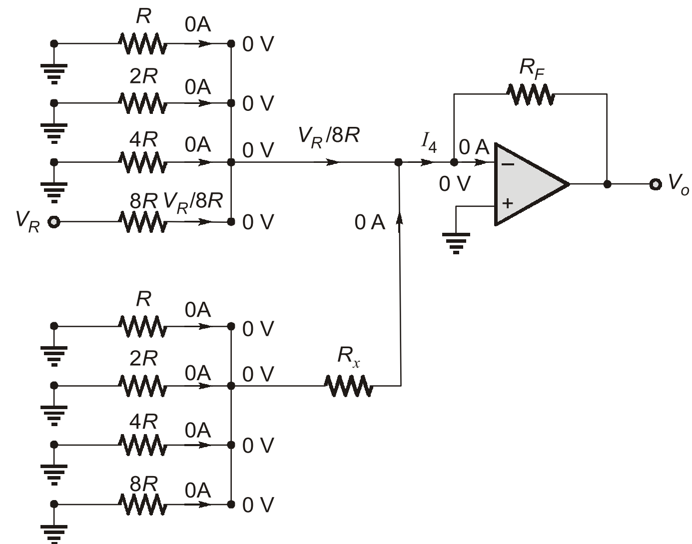
- Let, $I_{in} = I_0$ when $(b_7 \ldots b_0) = (0000\ 0001)$
  and $I_{in} = I_4$ when $(b_7 \ldots b_0) = (0001\ 0000)$

$$(0000\ 0001)_2 = (1)_{10} \text{ and } (00010000)_2 = (16)_{10}$$

So, $$I_4 = 16I_0 \quad \ldots(i)$$

To calculate I_4 :

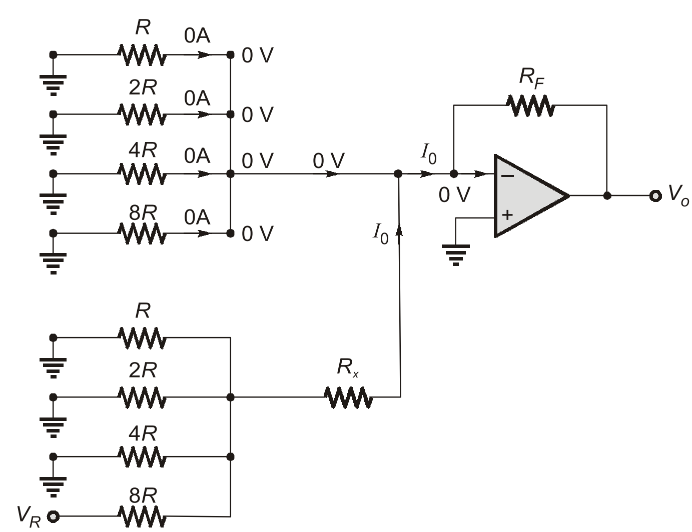
- When $(b_7 \ldots b_0) = (0001\ 0000)$, the given circuit can be equivalently drawn as,



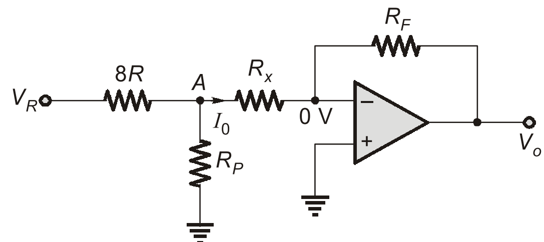
So, $$I_4 = \frac{V_R}{8R} \quad \ldots(ii)$$

To calculate I_0 :

- When $(b_7 \ldots b_0) = (0000\ 0001)$, the given circuit can be equivalently drawn as,



- The above circuit can be further reduced as,



By applying KCL at node 'A', we get,

$$\frac{V_R - V_A}{8R} = \frac{V_A}{R_P} + \frac{V_A - 0}{R_x} \; ; \; R_P = R \parallel 2R \parallel 4R = \frac{4R}{7}$$

$$V_A\left(\frac{1}{8R} + \frac{7}{4R} + \frac{1}{R_x}\right) = \frac{V_R}{8R}$$

$$V_A(R_x + 14R_x + 8R) = V_R R_x$$

$$V_A = \frac{V_R R_x}{8R + 15R_x}$$

and,
$$I_0 = \frac{V_A - 0}{R_x} = \frac{V_A}{R_x} = \frac{V_R R_x}{R_x(8R + 15R_x)} \quad \text{...(iii)}$$

- From equations (i), (ii) and (iii),

$$\frac{V_R}{8R} = 16\left[\frac{V_R R_x}{R_x(8R + 15R_x)}\right]$$

$$15R^2_x + 8RR_x = 128RR_x$$

$$15R_x = 120R$$

$$R_x = 8R$$

- So, when $R_x = 8R$, the given circuit can be used as an 8-bit (binary) digital-to-analog converter.

(ii) When the given circuit is used as a 2-decade BCD digital-to-analog converter,

$$I_4 = 10I_0 \quad \text{...(iv)}$$

- From equations (ii), (iii) and (iv), we get,

$$\frac{V_R}{8R} = 10\left[\frac{V_R R_x}{R_x(8R + 15R_x)}\right]$$

$$15R_x^2 + 8RR_x = 80\,RR_x$$

$$15R_x = 72R$$

$$R_x = \frac{72}{15}R = 4.8R$$

- So, when $R_x = 4.8\,R$, the given circuit can be used as a 2-decade BCD digital-to-analog converter.

7.1.3 The Switched-Capacitor Type DAC

The switched-capacitor type DAC employs weighted capacitors instead of weighted resistors. In this method, charged capacitors form a capacitive voltage divider whose output is proportional to the sum of the binary inputs.

Q.12 In a standard 4-bit flash type ADCs total number of resistors connected are
(a) 4 (b) 15
(c) 6 (d) 8

Q.13 Consider an n-bit slowest Dual-slope type ADC having conversion time 't_c' equals to 2 msec is clocked with 16 kHz pulses, then this ADC converts a binary sequence of
(a) 4-bits (b) 5-bits
(c) 6-bits (d) 16-bits

Q.14 The ratio of maximum conversion time of 8 bit digital ramp type ADC to that of 8 bit successive approximation type is
(a) 256 (b) 32
(c) 8 (d) 2

Q.15 Consider a 6-bit digital ramp ADC having clock frequency is 1 MHz. If a DAC has full scale output is 10.2 V and a threshold voltage of comparator is V_T = 4 mV.

(*i*) The digital binary equivalent for an input voltage of 3.5 volts will be
(a) 001011 (b) 010110
(c) 011011 (d) 001110

(*ii*) For the above statement, the conversion time to reach this value equals to
(a) 21.95 μsec (b) 10.98 μsec
(c) 13.92 μsec (d) 26.97 μsec

Q.16 An 8-bit ADC with a full-scale output voltage of 8.5 V is designed to have a $\pm\frac{1}{2}$ LSB accuracy. If the ADC is calibrated at 25°C and operating temperature ranges from 0°C – 50°C, then maximum net temperature coefficient of ADC should not exceed
(a) ±977 μV/°C (b) ±1953 μV/°C
(c) ±1000 μV/°C (d) ±1450 μV/°C

Q.17 In a tracking-type A/D converter a 5 MHz clock pulse is to applied to convert a single analog input to a digital output sequence 01101110. Required average conversion time is
(a) 51 μsec (b) 25.5 μsec
(c) 102 μsec (d) 12.8 μsec

Answer Key:

1. (d)	**2.** (c)	**3.** (d)	**4.** (b)	**5.** (d)
6. (b)	**7.** (*i*) (a) & (*ii*) (c)		**8.** (b)	**9.** (d)
10. (d)	**11.** (c)	**12.** (c)	**13.** (a)	**14.** (b)
15 (*i*) (b)	**15** (*ii*) (a)	**16.** (b)	**17.** (b)	

■■■■