POSTAL Book Package 2021

Computer Science & IT

Objective Practice Sets

Digital Logic

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3 CHAPTER

Logic Gates and Switching Circuits

Q.1 Which of the following expressions is not equivalent to $\bar{x}$?

(a) x NAND x (b) x NOR x

(c) x NAND 1 (d) x NOR 1

Q.2 $Y = f(A, B) = \Pi M(0, 1, 2, 3)$ represents (M is Maxterm)

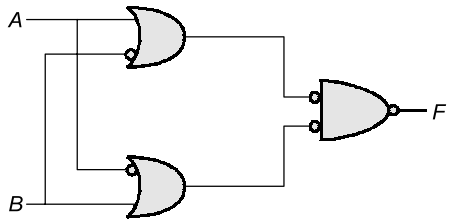
(a) NOR gate

(b) NAND gate

(c) OR gate

(d) a situation where output is independent of input

Q.3 The Boolean expression corresponding to the given circuit



(a) is independent of A

(b) is an inconsistency

(c) is a tautology

(d) none of these

Q.4 Consider $Y = A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A$ then Y is equivalent to:

(a) 1 OR A (b) A EXOR 0

(c) 1 NOR $\bar{A}$ (d) A AND A

Q.5 If the output of a logic gate is 1, when all its inputs are at logic '0', the gate is either

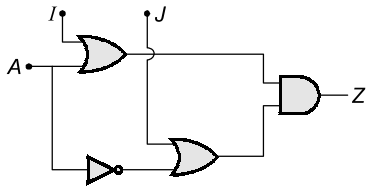
(a) a NAND or a NOR

(b) AND or an EX-OR

(c) an OR or a NAND

(d) an EX-OR or an EX-NOR

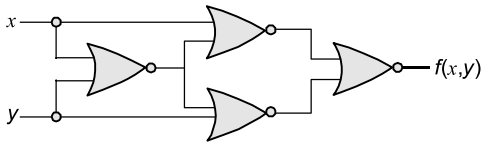
Q.6 The circuit shown below is to be used to implement the function $Z = f(A, B) = \bar{A} + B$. The values of I and J are



(a) $I = 0$ and $J = B$ (b) $I = 1$ and $J = B$

(c) $I = B$ and $J = 1$ (d) $I = B$ and $J = 0$

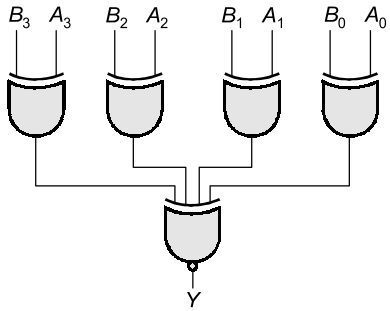
Q.7 Identify the logic function performed by the circuit shown in the given figure



(a) exclusive OR (b) exclusive NOR

(c) NAND (d) NOR

Q.8 A digital circuit which compares two numbers $A_3\ A_2\ A_1\ A_0$, $B_3\ B_2\ B_1\ B_0$ is shown in figure. To get output $Y = 0$, choose one pair of correct input numbers.



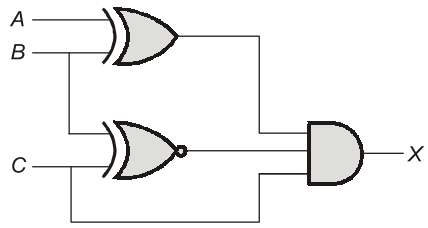
(a) 1010, 1010 (b) 0101, 0101

(c) 0010, 0010 (d) 1010, 1011

Q.9 Statement (I): XOR gate a not a universal gate.
Statement (II): It is not possible to realise any Boolean function using XOR gates only.

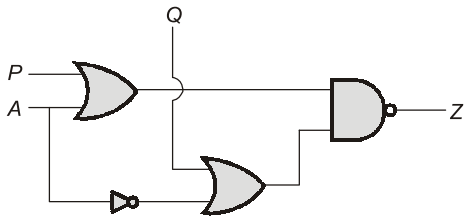
(a) Both statement (I) and statement (II) are individually true and statement (II) is the correct explanation of statement (I).
(b) Both statement (I) and statement (II) are individually true but statement (II) is not the correct explanation of statement (I).
(c) Statement (I) is true but statement (II) is false.
(d) Statement (I) is false but statement (II) is true.

Q.10 Which of the input condition (*ABC*) produces $X = 1$ in the logic circuit shown below?



(a) 101 (b) 011
(c) 111 (d) 110

Q.11 The circuit shown below is used to implement the functions $Z = f(A,B) = \overline{A} + B$. The values of *P* and *Q* are

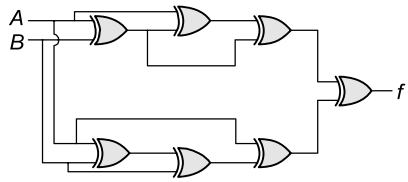


(a) $P = A,\ Q = B$ (b) $P = B,\ Q = \overline{A}$
(c) $P = \overline{B}, Q = 0$ (d) $P = 0, Q = \overline{B}$

Q.12 The minimum number of NAND gates required to implement the boolean function $ABCDE + ABCD + ABC + AC + C$ is

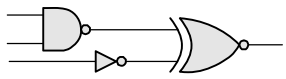
(a) 0 (b) 1
(c) 4 (d) 7

Q.13 The output '*f*' of the given circuit is _____.

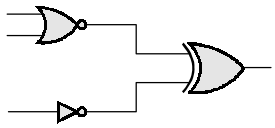


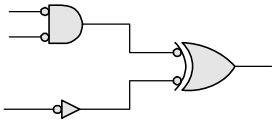
(a) 0 (b) 1
(c) *A* (d) *B*

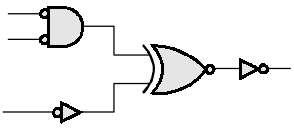
Q.14 A positive level logic digital circuit is shown below:



The negative level logic digital circuit for the given circuit is

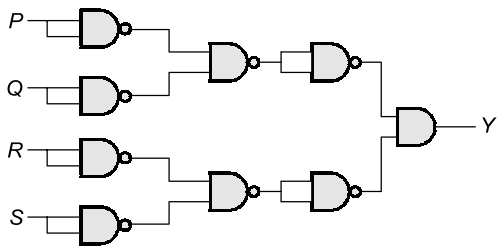
(a) 

(b) 

(c) 

(d) All of these

Q.15 For the circuit shown in figure the Boolean expression for the output *Y* in terms of inputs *P*, *Q*, *R* and *S* is



(a) $\overline{P} + \overline{Q} + \overline{R} + \overline{S}$
(b) $\overline{P}\,\overline{Q}\,\overline{R}\,\overline{S}$
(c) $(\overline{P} + \overline{Q}) + (\overline{R} + \overline{S})$
(d) $(P + Q)\,(R + S)$

Answers Logic Gates and Switching Circuits

1.	(d)	2.	(d)	3.	(c)	4.	(b)	5.	(a)	6.	(b)	7.	(b)	8.	(d)	9.	(a)
10.	(b)	11.	(d)	12.	(a)	13.	(c)	14.	(d)	15.	(b)	16.	(b)	18.	(a)	19.	(a)
21.	(a)	23.	(c)	26.	(c)	29.	(d)	30.	(d)	31.	(a)	34.	(a)	35.	(d)	39.	(d)

Explanations Logic Gates and Switching Circuits

1. (d)

x NAND x = $\overline{x \cdot x} = \bar{x}$

x NOR x = $\overline{x + x} = \bar{x}$

x NAND 1 = $\overline{x.1} = \bar{x}$

x NOR 1 = $\overline{x+1} = 0$

Hence, (d) is the required option.

2. (d)

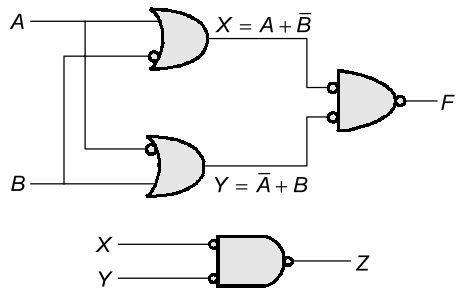
$$Y = f(A, B) = \Pi M(0, 1, 2, 3)$$

K-map for Y:

$Y = 0$, which represents a situation where output is independent of input.

B \ A	0	1
0	0	0
1	0	0

3. (c)



$$Z = \overline{\bar{X} \cdot \bar{Y}} = X + Y$$

$$\Rightarrow \quad F = A + \bar{B} + \bar{A} + B = 1$$

So F is a tautology.

4. (b)

$y = A \oplus (\bar{A} \oplus \bar{A}) \oplus (A \oplus A) \oplus (\bar{A} \oplus \bar{A}) \oplus (A \oplus A)$

Note: $A \oplus A = 0$

$A \oplus \bar{A} = 1$

$\therefore \quad Y = A \oplus 0 \oplus 0 \oplus 0 \oplus 0 = A \oplus 0$

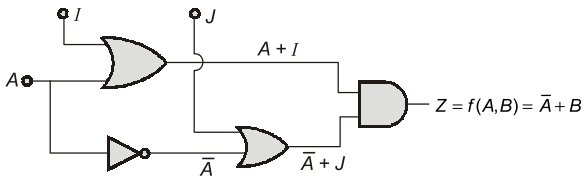
Hence $Y = A$ EXOR 0

Hence (b) is correct option.

5. (a)

NAND and NOR gates give output as 1 when all inputs are 0.

6. (b)



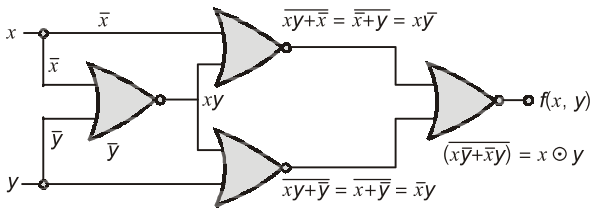
$$Z = (A + I)(\bar{A} + J)$$

Put, $I = 1$; $J = B$

$$Z = (A + 1)(\bar{A} + B)$$

$$Z = (\bar{A} + B)$$

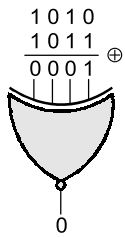
7. (b)



Therefore the above circuit performed exclusive NOR gate.

8. (d)

In EX-NOR gate, if odd number of inputs are 1 then output is zero.



9. (a)

A gate is said to be universal if all logic functions possible in the given number of variables can be realised using that particular gate.

Since all functions can not be realised using XOR gates alone, therefore it is not a universal gate.

Note: NAND and NOR gates are universal gates.

10. (b)

$X = 1$ occurs when all inputs to the AND gate are at logic 1.

$\therefore \quad C = 1$

$A \oplus B = 1$

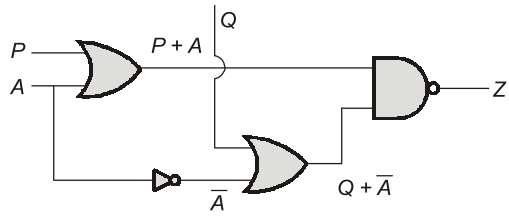
$B \odot C = 1$

Since $C = 1$, $\therefore B \odot C = 1$ when $B = 1$

Since $A \oplus B = 1$, $\therefore A = 0$

$(ABC) = (011)$

11. (d)



$$Z = \overline{(P+A)(Q+\bar{A})}$$

$$= (\overline{P+A}) + (\overline{Q+\bar{A}})$$

$$= \bar{P}\bar{A} + \bar{Q}A$$

If $P = 0, Q = \bar{B}$, $Z = \bar{0}.\bar{A} + B.A$

$$= \bar{A} + AB$$

$$[\because \bar{0} = 1, 1.A = A]$$

$$= \bar{A} + B$$

12. (a)

$ABCDE + ABCD + ABC + AC + C$

$= ABCD\,(1 + E) + AC(B + 1) + C$

$= ABCD + AC + C$

$= ABCD + (A + 1)C$

$= ABCD + C$

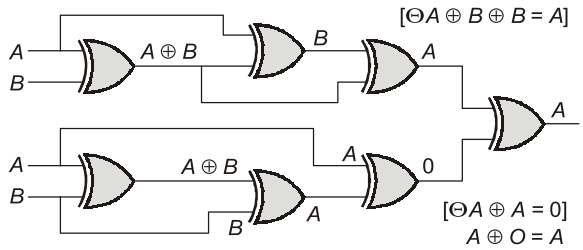
$= C(1 + ABD)$

$= C(1 + A)\,(1 + B)\,(1 + D)$

$= C$

$\therefore$ 0 gates are required.

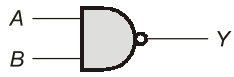
13. (c)



14. (d)

The negative level logic circuit is a dual circuit of positive level logic circuit.

Using dual logic gates, it can be shown that the circuits in option (a), (b) and (c) are all same in operation.

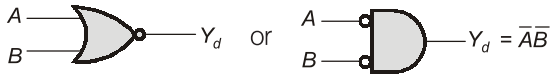
For a NAND gate 

$$Y = \overline{AB}$$

The dual of Y will be

$$Y_d = \overline{(A+B)}$$

which can be obtained by



For a XOR gate 

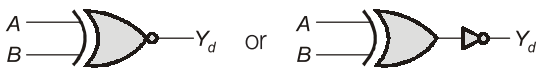
$$Y = A \oplus B$$

$$= \bar{A}B + A\bar{B}$$

The dual of Y will be

$$Y_d = (\bar{A} + B)(A + \bar{B}) = A \odot B$$

Which can be obtained by



15. (b)

$$Y = \overline{(\bar{P}\cdot\bar{Q})}\cdot\overline{(\bar{R}\cdot\bar{S})} = P\,Q\,R\,S$$

16. (b)

Take two or three input '1' then we always get '1'

or

Take two or three input zero then we always get '0' hence option '*b*' is true and output

$$Y = PQ + PR + RQ$$

Note: This is also known as the majority function.

By simplifying the above circuit

$$Y = \overline{\overline{PQ}.\overline{QR}.\overline{PR}}$$

$$= \overline{\overline{PQ}.\overline{QR}.\overline{PR}}$$

$$= PQ + QR + PR$$

17. (20)

Consider a single NOT gate in feedback circuit. In 1 propagation delay (i.e., 2 ns) we get $1 \rightarrow 0$ where 1 is the input. This 0 is fed as input to the NOT gate. After 1 more propagation delay we get the 0-1 in the time interval.

For n inverters in feedback circuit.

$T = 2n$ tpd where tpd is the propagation delay of 1 inverter.

$\therefore \quad T = 2 \times 5 \times 2 \times 10^{-9}\text{s} = 20 \text{ ns}$

18. (a)

$$Y = A(B + \bar{C}) + \bar{A}B + (A + \bar{B})C$$

$$= AB + A\bar{C} + \bar{A}B + AC + \bar{B}C$$

$$= (AB + \bar{A}B) + (A\bar{C} + AC) + \bar{B}C$$

$$= (A + \bar{A})B + A(C + \bar{C}) + \bar{B}C$$

$$[\because A + \bar{A} = 1; A.1 = A]$$

$$= B + A + \bar{B}C$$

$$= A + \bar{B}C + B \qquad [\because A + \bar{A}B = A + B]$$

$$= A + B + C$$

19. (a)

When $Y = 1$, the XOR gate behaves as a NOT gate n NOT gates or inverters connected in feedback produces an oscillation with time period.

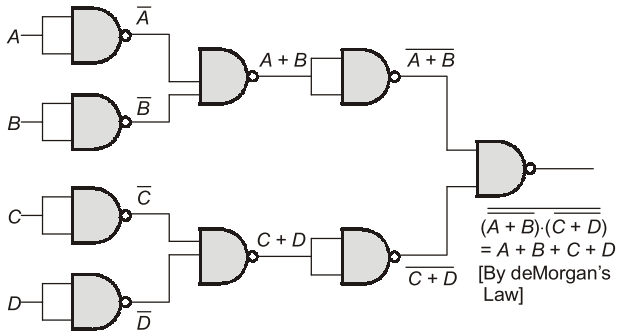
$$T = 2n \text{ tpd}$$

where tpd is the propagation delay.

Note that n must be odd to obtain oscillating signal.

20. (9)

$$A + B + C + D = \overline{\bar{A}.\bar{B}.\bar{C}.\bar{D}}$$



21. (a)

Coincidence logic is the EX-NOR logic.

Required logic is $\bar{A}\bar{B} + AB$

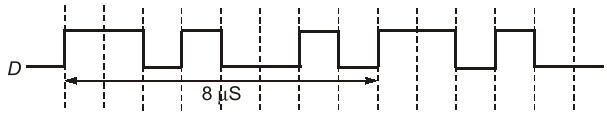
In (a) $F = AB + \bar{A}\bar{B}$

22. (125)

The function represented by the circuit is

$$Y = A \odot B \odot C$$

$$= A \oplus B \oplus C$$



The time period of the output is 8 μs

$$f = \frac{1}{T} = \frac{1}{8 \times 10^{-6}}$$

$$= 0.125 \times 10^6 \text{ Hz} = 125 \text{ kHz}$$

23. (c)

$$f(w, x, y, z) = f_1 \cdot f_2 + \bar{f}_3$$

Let $\bar{f}_3 = f_4$

$$f_1 = w\bar{x}z + y\bar{z} + x\bar{z}$$

wx \ yz	00	01	11	10
00				1
01	1			1
11	1			1
10		1	1	1

$\therefore \quad f_1 = \Sigma m(2, 4, 6, 9, 10, 11, 12, 14)$

$f_2 = \Sigma m(6, 9, 12) + d(0, 1, 3, 5, 7, 8, 13)$

[$\because$ The desired minterms in f must be present in both f_1 and f_2.]