POSTAL Book Package

2021

Electronics Engineering

Conventional Practice Sets

Electronic Devices and Circuits

| ςι | Topic | Page No. |
|-------------|--------------------------------------|----------|
| J 1. | ТОРІС | rage No. |
| 1. | Basic Semiconductor Physics | 2 - 15 |
| 2. | PN Junction and Circuits | 16 - 36 |
| 3. | Bipolar Junction Transistor | 37 - 57 |
| 4. | Field Effect Transistor | 58 - 71 |
| 5. | Power Switching Devices and Circuits | 72 - 77 |
| 6. | Introduction to IC Fabrication | 78 - 80 |





Note: This book contains copyright subject matter to MADE EASY Publications, New Delhi. No part of this book may be reproduced, stored in a retrieval system or transmitted in any form or by any means.

Violators are liable to be legally prosecuted.



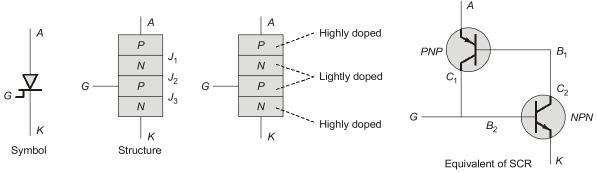
Power Switching Devices and Circuits

Practice Questions: Level-I

Q1 What are SCRs? Draw the symbol and its *V-I* characteristics. Explain its operation.

Solution:

- SCR is a thyristor family member.
- SCR is a 4 layer solid state device with 3 terminals (A, K and G) and having 3 junctions.
- Unidirectional device.



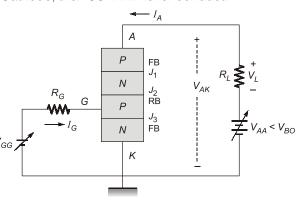
- In SCR internal regions are relatively lightly doped when compared to outermost layer.
- The equivalent circuit of SCR can be represented by one PNP transistor and one NPN transistor connected back to back.
- SCR is a latch.
- Bi-stable device i.e. having stable ON and OFF states.
- SCR can handle large amount of power with a very small amount of power consumption.
- If anode is given a negative voltage with respect to Cathode, then SCR will never conduct.

Current operation of SCR:

Also called Gate operation of SCR

If I_{G} is kept zero and let $\textit{V}_{\textit{AA}} < \textit{V}_{\textit{BO}}$

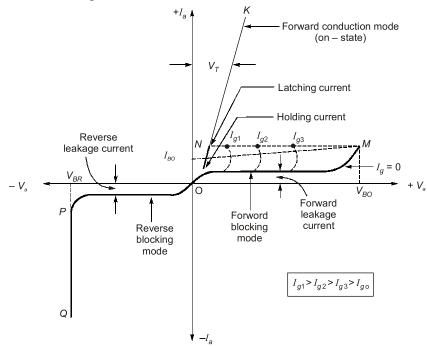
- Junctions J_1 and J_3 are FB and J_2 is RB.
- Internal resistance of SCR is very large ($\geq 1 \text{ M}\Omega$).
- The function of Gate is trigger the SCR by sending a proper I_G.
- Once SCR is triggered by sending proper I_G , the SCR will be loosing total control on I_A and SCR will continue to remain is ON STATE.
- Once SCR is ON, it will not respond to the Gate.
- SCR can be switched OFF by using any one of the following methods:
 - (i) Disconnect V_{AA} .
 - (ii) Give anode Anode a negative voltage with respect to cathode.
 - (iii) Reduce V_{AA} so that I_A reduces and falls below certain value of current I_H (Holding current) and SCR will go to OFF.





The firing voltage of SCR $\propto \frac{1}{I_G}$ i.e. by applying larger values of I_G we can trigger the SCR.

VI characteristic of SCR is given below:

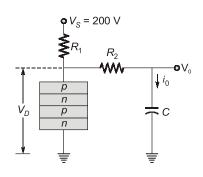


Use the device to design a simple circuit to generate a continuous sawtooth wave of amplitude 100 volts, and repetitive frequency of 500 Hz. The following data is available regarding the four layer diode: $V_{BO} = 100 \text{ V}, I_A = 20 \text{ A}, I_H = 20 \text{ mA}.$

Solution:

The circuit to generate a continuous sawtooth wave using a four layer p-n-p-n diode is shown here.

When the diode is OFF, it is effectively open and capacitor C charges to 200 V through R_1 & R_2 . When $V_D = V_0$ reaches V_{BO} (= 100 V), the diode turns ON and acts like a (say 1 $V = V_H$) battery. The capacitor now discharges to V_H through R_2 . When $i_D = i_0$ reaches the holding current $I_H = 20$ mA, the diode switches off and C begins to charge again also, I_A = 20 A.



When diode is ON:

$$V_0 = V_{\infty} - (V_{\infty} - V_1) e^{-t/T_{ON}}$$
 where
$$V_{\infty} = 1 \text{ V and } V_1 = 100 \text{ V}$$
 ...(i)
$$V_0 = 1 + 99 e^{-t/T_{ON}}$$
 ...(i)
$$T_{ON} = R_2 C$$

$$T_{ON} = R_2 C$$

$$T_{ON} = C \frac{dV_0}{dt}$$

$$V_{BO} \approx 100 \text{ V}$$
 OFF ON
$$V_{BO} \approx 100 \text{ V}$$
 At
$$t = T_2, i_0 = -20 \times 10^{-3} \text{ A} \text{ (Given)}$$



When diode is OFF:

$$V_0 = V_{\infty} - (V_{\infty} - V_1) e^{-t/T_{OFF}}$$
 where
$$V_{\infty} = 200 \text{ V and } V_1 = 1.1 \text{ V}$$

$$T_{OFF} = (R_1 + R_2)C \approx RC$$
 At
$$t = T_1, V_0 = 100 \text{ V}$$

$$\therefore \qquad \text{Repetitive frequency} = f = \frac{1}{T_1 + T_2} = 500 \text{ Hz}$$

After solving all the above equations we get,

$$R_1 = 1 \text{ M}\Omega$$
, $R_2 = 100 \Omega$ and $C = 5 \mu\text{F}$.

Q3 For an SCR, the gate cathode characteristic has a straight-line slope of 130. For trigger source voltage of 15 volt and allowable gate power dissipation of 0.5 watts. Determine the Gate-source resistance?

Solution:

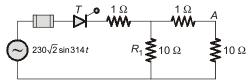
Here given that,
$$Power = V_g I_g = 0.5 \text{ Watt} \\ \frac{V_g}{I_g} = 130 \\ \dots (ii)$$
 So,
$$130 \ I_g^2 = 0.5 \\ \text{or} \\ I_g^2 = \frac{0.5}{130} \\ \text{or} \\ I_g = \sqrt{3.846 \times 10^{-3}} = 0.062 \text{ A} \\ \frac{I}{g} = 62 \text{ mA} \\ \text{So, gate voltage} = V_g = 130 \ I_g \\ \Rightarrow V_g = 8.06 \text{ volt} \\ \text{In the SCR, for the Gate circuit we have,} \\ E_s = I_g R_s + V_g = 0.062 \times R_s + 8.06 \\ \end{bmatrix}$$

or

or
$$\frac{15 - 8.06}{0.062} = R_s$$

Gate-source resistance ($R_{\rm s}$) = 111.94 Ω

Q4 Thyristor shown in the figure has I^2t rating of 20 A² sec. If terminal 'A' get short circuited to the ground. Calculate the fault clearance time so that SCR is not damaged.



Solution:

The worst possible fault current should be considered for calculating the fault clearance time. Maximum fault current occurs when source voltage is at its peak value = $230\sqrt{2}$ volt, when terminal 'A' gets shorted circuited to the ground, the resistance offered to source is equal to,

$$\frac{10 \times 1}{11} + (1) = \frac{21}{11} \Omega$$

Assuming maximum fault current = $\frac{230\sqrt{2} \times 11}{21}$ A, which is to remain constant during the short clearance time (t_c) we get,



or

 \Rightarrow

$$\int_{0}^{t_{c}} i^{2} dt = \int_{0}^{t_{c}} \left(\frac{230\sqrt{2} \times 11}{21} \right)^{2} \cdot dt = 20 \text{ A}^{2}$$

$$t_{c} = 20 \left[\frac{21}{230\sqrt{2} \times 11} \right]^{2} \times 1000 \text{ ms}$$

$$t_{c} = 0.6892 \text{ m-sec}$$

Practice Questions: Level-II

Q5 For an SCR, gate-cathode characteristic is given by the equation,

$$V_a = 1 + 10 I_a$$

 V_g = 1 + 10 I_g The Gate source voltage is a rectangular pulse of 15 V with 20 μ -sec duration. For an average gate power dissipation of 0.3 Watt and a peak gate-drive power of 5 Watt.

- (a) the resistance to be connected in series with the SCR gate.
- (b) the triggering frequency.
- (c) the duty cycle of the triggering pulse.

Solution:

(a) For an SCR, we have given,

$$V_g = 1 + 10 I_g$$
 ...(i)

For pulse-triggering of SCRs during pulse-on period, we have

(peak-gate voltage)
$$\times$$
 (peak-gate current) = peak-gate drive power i.e. P_{am} ...(ii)

As the gate rectangular pulse width is 20μ -sec (i.e. less than 100μ -sec), so there is no any dc data will be applicable. Had the gate pulse width been more than 100 μ-sec, the relation given,

$$\begin{aligned} V_g &= 1 + 10\,I_g \\ V_g \times I_g &= (1 + 10\,I_g)\,I_g \end{aligned}$$

 \Rightarrow 10 $I_g^2 + I_g = 0.3$ Watt, will holds good but as the dc data not applied here, we should note that:

$$(1 + 10 I_g) \times I_g = 5$$

$$\Rightarrow 10 I_g^2 + I_g - 5 = 0 \qquad ...(iii)$$

$$\therefore I_g = 0.659 \text{ A or } -0.759 \text{ A}$$

So, we get the value of $I_a = 0.659$ A

Hence, amplitude of the current pulse = 0.659 A

Now, during the pulse-ON period,

$$E_{s} = I_{g} + I_{g} \cdot R_{s}$$

$$= I_{g}R_{s} + (10 I_{g} + 1)$$

$$\Rightarrow R_{s} = \frac{E_{s} - V_{g}}{I_{g}} = \frac{15 - 1 - (10 \times 0.659)}{0.659}$$

$$\therefore R_{s} = 11.24 \Omega$$
[From equation (i)]

(b) Since,
$$P_{gm} = \frac{P_{gaV}}{fT}$$
 [Here, $T = 20 \,\mu\text{-sec}$]

and Triggering frequency (f) =
$$\frac{P_{gaV}}{T \times P_{gm}}$$

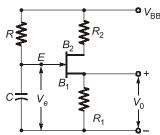
$$\Rightarrow \qquad f = \frac{0.3 \times 10^6}{20 \times 5} = 3 \text{ kHz}$$

(c) Duty cycle =
$$d = fT = 3 \times 10^3 \times 20 \times 10^{-6} = 0.06$$



Q.6 A relaxation oscillator using an UJT as shown in figure below, is to be designing for triggering of an SCR. The data of an UJT is

η = 0.72, $I_P = 0.6$ mA, $V_P = 18$ V, $V_V = 1$ V, $I_V = 2.5$ mA, $R_{BB} = 5$ kΩ, normal leakage current with emitter open = 4.2 mA, firing frequency is 2 kHz. Then for C = 0.04 μF, determine the value of R, R_1 and R_2 .



Solution:

In an UJT, the time required (T) for a capacitor (C) to charge from initial voltage ' V_{v} ' to peak point voltage ' V_{p} ' through a large resistor 'R' can be obtained as:

$$T = \frac{1}{f} = RC \ln\left(\frac{1}{1-\eta}\right) \qquad \dots(i)$$

$$R = \frac{1}{fC \ln\left(\frac{1}{1-\eta}\right)} = \frac{10^6}{2000 \times 0.04 \times \ln(3.57)}$$

$$\therefore \qquad R = 9.82 \text{ k}\Omega$$

As, V_D is not given so,

$$V_{\rho} = \eta \ V_{BB}$$

$$V_{BB} = \frac{V_{\rho}}{\eta} = \frac{18}{0.72} = 25 \text{ V}$$
we know that,
$$R_{2} = \frac{10^{4}}{\eta V_{BB}} = \frac{10^{4}}{0.72 \times 25} = 555.5 \ \Omega$$

As given that, emitter is open,

So,
$$V_{BB} = \text{normal leakage current } (R_1 + R_2 + R_{BB})$$

$$\Rightarrow R_1 + R_2 + R_{BB} = \frac{25 \times 10^3}{4.2} = 5.95 \times 10^3 \,\Omega$$

$$\Rightarrow R_1 = (5952.38 - 5000 - 555.5) \,\Omega$$

$$\therefore R_1 = 397 \,\Omega$$

What are Opto-isolators? Where do they find application? Discuss their propagation delay, operating voltage range and power dissipation.

Solution:

The opto-isolators which is also called opto-coupler are the device which are optically coupled but electrically isolated that incorporate many characteristics.

⇒ A schematic arrangement of opto-coupler is given below:

